Lochnagar 2

User Guide

For firmware version 1.5.1

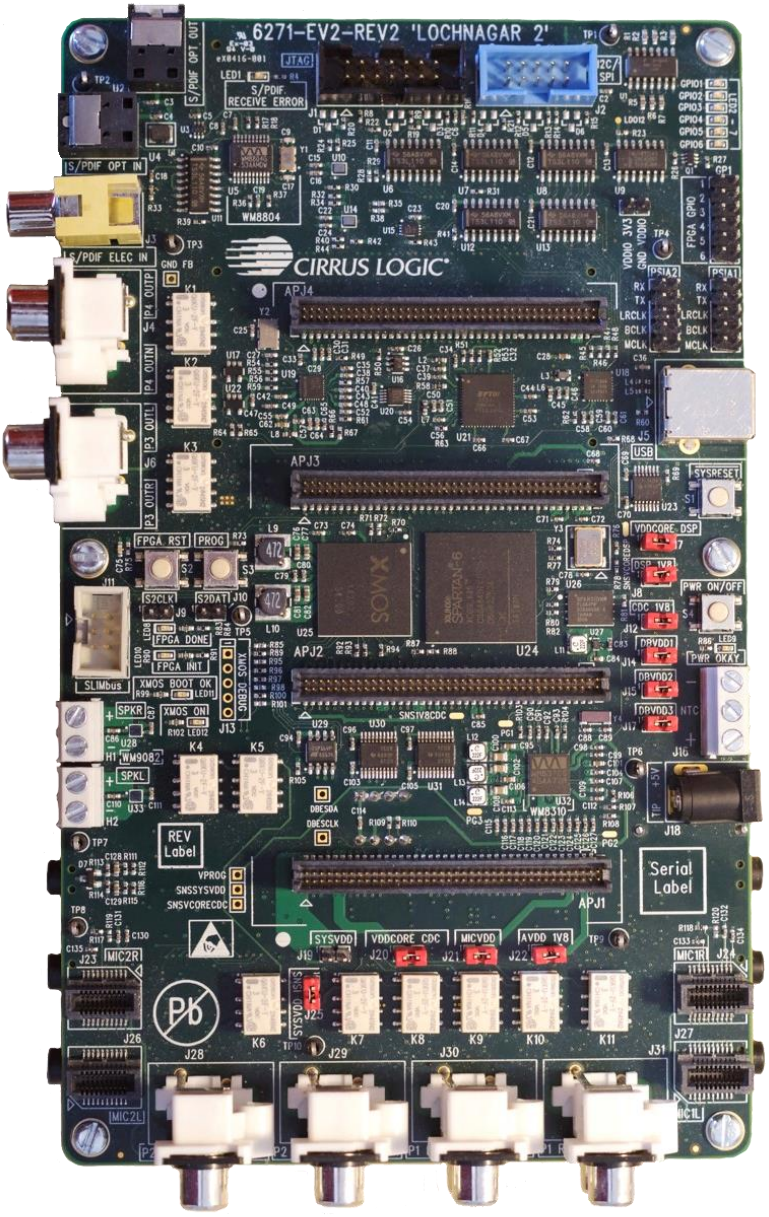


Table of Contents

1 Introduction

Lochnagar 2 (6271-EV2) is the next generation evaluation and development board for Cirrus Logic Smart Codec and Amps devices. It is designed to provide a variety of audio inputs and outputs to Cirrus Logic devices and to allow for configuration and programming them in a variety of possible use cases.

Lochnagar 2 is the same form factor as the original Lochnagar board and is compatible with the same Smart Codec and Amp minicards. It provides all the same functionality as the previous generation, and in addition adds many new features and capabilities. This includes the ability to stream up to 16 channels of USB audio, and a built-in current monitor feature that allows the power consumption of Cirrus Logic devices to be measured without any external equipment.

This document describes the features and usage of Lochnagar 2 in detail. The first two sections deal with the initial steps of hardware configuration and driver installation. Subsequent sections detail each of the features of the board and how to set it up in any potential use case. The final sections detail how to use the setup scripts provided with the Lochnagar 2 Device Pack and a guide on troubleshooting the board if any problems occur.

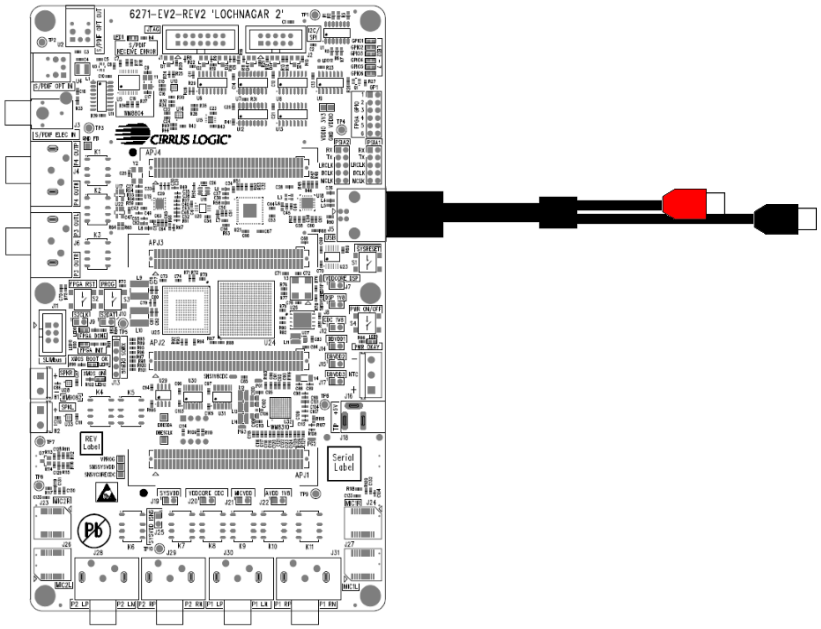
2 Hardware Connections

2.1 USB Connection

Lochnagar 2 is powered and controlled via a single USB connection. This provides:

- Power
- I2C/SPI communications to control device and board
- JTAG communications for DSP debug
- Multichannel USB streaming audio (USB class 2)
- USB serial port to communicate with Cirrus Logic devices with UART interfaces

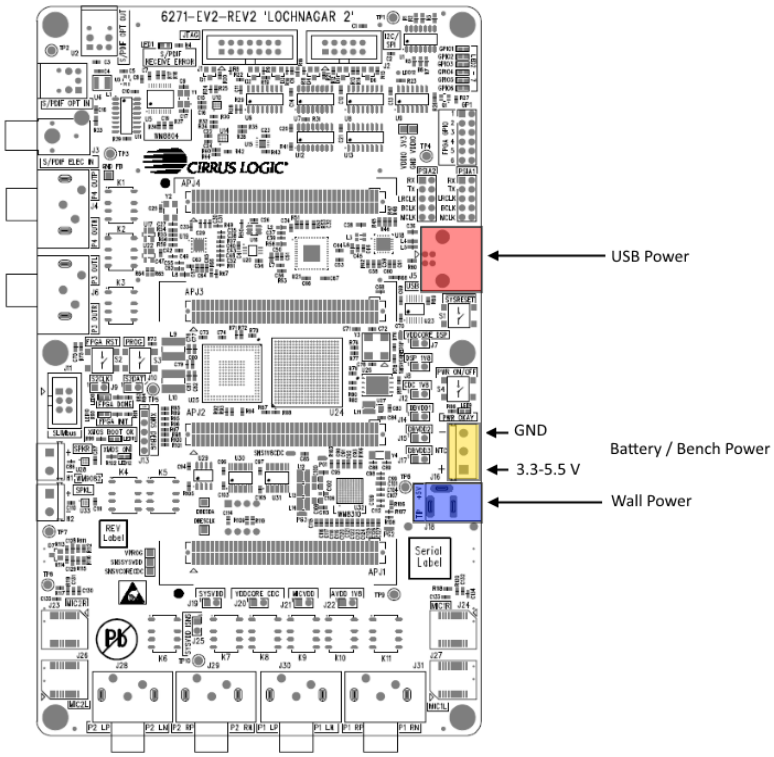
The board is provided with a Y-shaped USB cable, connecting a single USB B socket on Lochnagar 2 to two USB A ports on the computer (the black plug is for power and communications, the red for power only). Both USB connectors must be plugged in to allow for the power consumption of the board.



A Total Phase Aardvark connector is **NOT** required for Lochnagar 2 to operate, neither is a separate power supply required. All power and communications is provided to the board via this single USB link.

2.2 Power Options

For most use cases, the provided USB cable is enough to power the entire board. In some scenarios, especially those using speakers, it may be necessary to plug a second power source into the Lochnagar 2 board. The onboard WM8310 PMIC will select the highest voltage from each of the three potential power supply inputs and use this to power the board's main SYSVDD bus. This is nominally 5V, but may be lower if a battery is used to supply the board.



2.2.1 USB Power

As described in the USB Connection section, this is the normal mode of operation for the Lochnagar 2 board. For most use cases, USB power alone is adequate and there is no need to connect any additional power supplies to the board.

To be certain of getting the full 900 mA maximum input current supported by Lochnagar 2 USB connection, it is vital to ensure that a Y-shaped dual-USB cable is used and that both ends are plugged in at the PC end. If a USB hub is used, then it is also important to use a self-powered USB hub with a wall power connection, as otherwise it may not be able to supply enough current.

2.2.2 Wall Socket Supply

Lochnagar 2 provides a socket to accept 5V input from a dedicated wall supply.
It may be necessary to plug in the wall supply as well as the USB connector for more power-hungry use-case scenarios such as those involving speakers.

The wall power connector J30 is positive tip (tip = +5V), in contrast to the original Lochnagar board which used negative tip.

Protection diodes are fitted to prevent damage if a negative tip supply is inserted.

2.2.3 Battery/Bench Supply

Lochnagar 2 has three screw terminals which allow either a battery or a bench-top power supply unit to be plugged into the board.

It may be necessary to plug in a bench supply as well as the USB connector for more power-hungry use-case scenarios such as those involving speakers.

This input is nominally expected to be a 4.2 V battery, but the terminals can accept anything from 3.3 – 5.5 V. The terminals are marked with + and - symbols on the silkscreen to denote power and ground respectively.

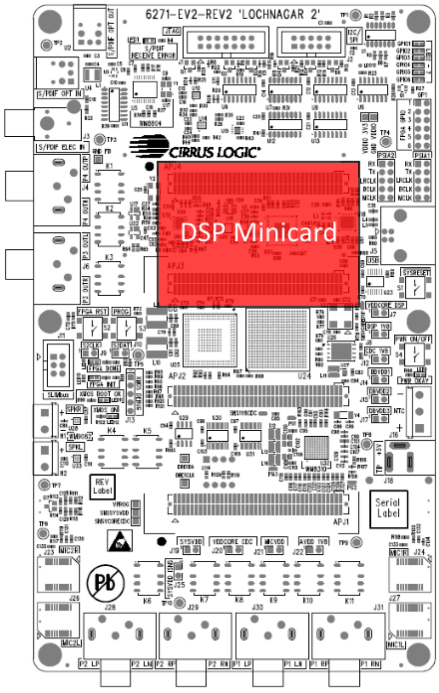
Note that when the battery/bench supply is used as the sole power source for the board, the PWR ON/OFF button (S4) must be held down in order to power the board. This is in contrast to the other supply options, where the board will automatically power on as soon as the wall or USB connector are plugged in.

2.3 Minicard Types

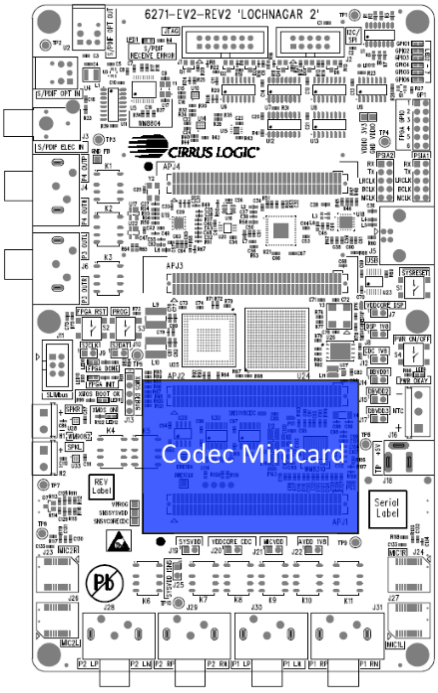
Lochnagar 2 works with interchangeable minicards to allow for a variety of Smart Codec devices. The minicard connectors are fully backwards compatible with the original Lochnagar board.

Minicards should not be inserted or removed while the Lochnagar 2 board is powered. If using the wall socket or battery/bench screw terminals for board power, then it is recommended to fully disconnect or power down the external supply before changing minicards.

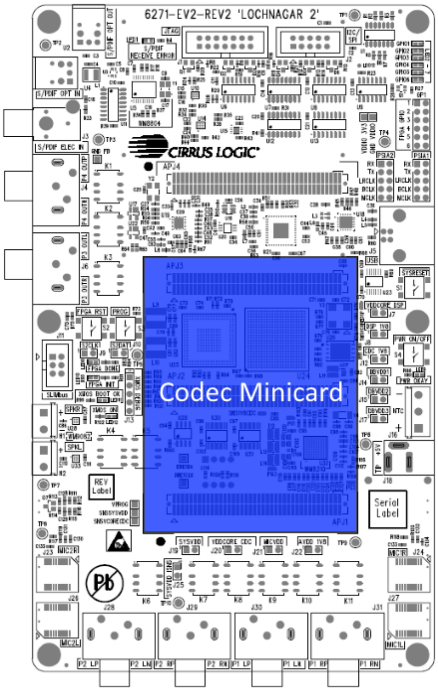
There are three main categories of minicard that can connect to Lochnagar 2.



DSP Minicard



Codec Minicard (2-Header)



Codec Minicard (3-Header)

2.3.1 DSP Minicard

This type of minicard was designed for an older range of sidecar DSPs that sit alongside a codec minicard.

DSP minicards connect to the top two headers on the Lochnagar 2 board.
There are no current product lines that use the DSP minicard slot.

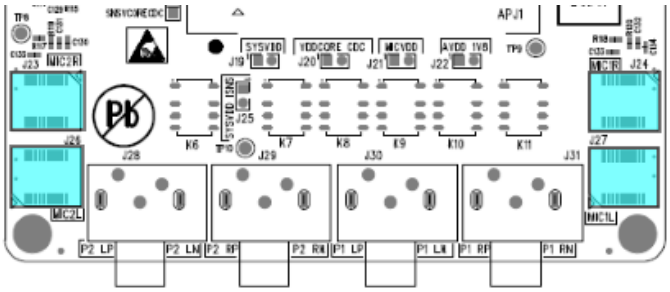
2.3.2 Codec Minicard

Codec minicards house Cirrus Logic Codec and Smart Codec type devices. Smart Codecs include a built-in DSP, but are not classed as "DSP" minicards.

Traditionally, codec minicards connect to the lower two headers on the Lochnagar 2 board. However, some of the larger Smart Codec devices extend to the third header in order to make use of the extra I/O. These cards cannot be used alongside a DSP minicard.

2.3.3 Microphone Minicards

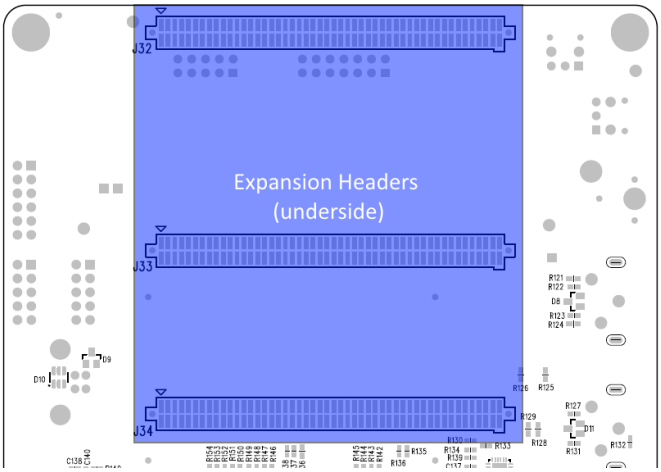
There are four microphone slots on the bottom of the Lochnagar 2 board.



These are designed to accept Cirrus Logic digital and analog microphone minicards.

2.4 Expansion Headers

There are three expansion headers on the underside of Lochnagar 2, as shown in **Error! Reference source not found.**. T hese are designed to connect the board to other test hardware. They are commonly used to connect Lochnagar 2 to a Linux Application Processor system.



2.5 Buttons/Switches

There are four push buttons on the Lochnagar 2 board connected with power and reset functionality.

Part Number	Name	Description
S1	SYSRESET	Resets all power rails on the board, returning all components to default state including Codec and FPGA
S2	FPGA RST	Resets all FPGA registers
S3	PROG	Resets FPGA operation, forcing a reprogram from EEPROM This will also reset all FPGA registers and re-initialize other components on the board
S4	PWR ON/OFF	Press when powered off: power on the board Hold down for 2 seconds when powered on: power off the board

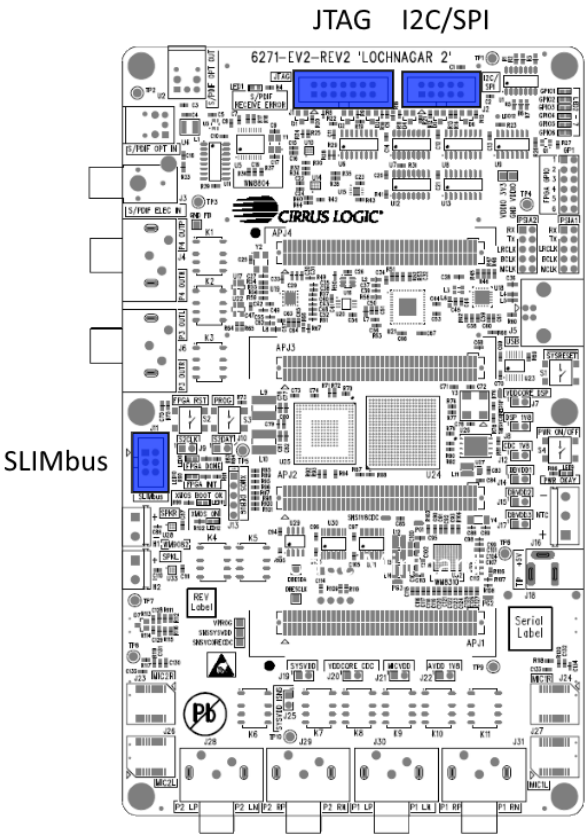
2.6 LED Indicators

There are six status LEDs on the Lochnagar 2 board that indicate the board's current state of operation:

Part Number	Color	Name	Normally Lit?	Description
LED1	Red	S/PDIF RECEIVE ERROR	No	Set to red when there is an error receiving S/PDIF signals
LED2-7	Green	GPIO1 - GPIO6	No	Tied to FPGA GPIOs 1 to 6.
LED8	Green	FPGA DONE	Yes	Indicates that the FPGA booted successfully
LED9	Green	PWR OK	Yes	Indicates the Lochnagar 2 board has power applied
LED10	Red	FPGA INIT	No	Indicates that the FPGA is currently initializing. Should flicker once upon board startup/power applied.
LED11	Green	XMOS BOOT OK	Yes	Indicates that the XMOS USB transceiver chip booted correctly
LED12	Green	XMOS ON	Yes	Indicates that the XMOS USB transceiver chip is powered

2.7 Other Headers

There are several other headers on the Lochnagar 2 board that allow for connections to other systems.



2.7.1 I2C/SPI (Aardvark)

Header J2 (I2C/SPI) is designed to connect to Total Phase Aardvark™ systems for legacy compatibility with the original Lochnagar board.

All I2C/SPI communications for most use cases are now expected to go through the standard USB link that also powers the board and provides USB audio streaming capability. However, the Aardvark can still be used for legacy applications or as a slave to test SPI master peripherals on the minicard.

2.7.2 JTAG

Header J1 (JTAG) is designed to connect to Macraigor usbWiggler™ JTAG systems for legacy compatibility with the original Lochnagar board.

As with the I2C/SPI communications, JTAG functionality is now possible using the standard USB link that also powers the board and provides USB Audio streaming. It is still possible to use the Macraigor through this header if required. USB is the default option within the register map.

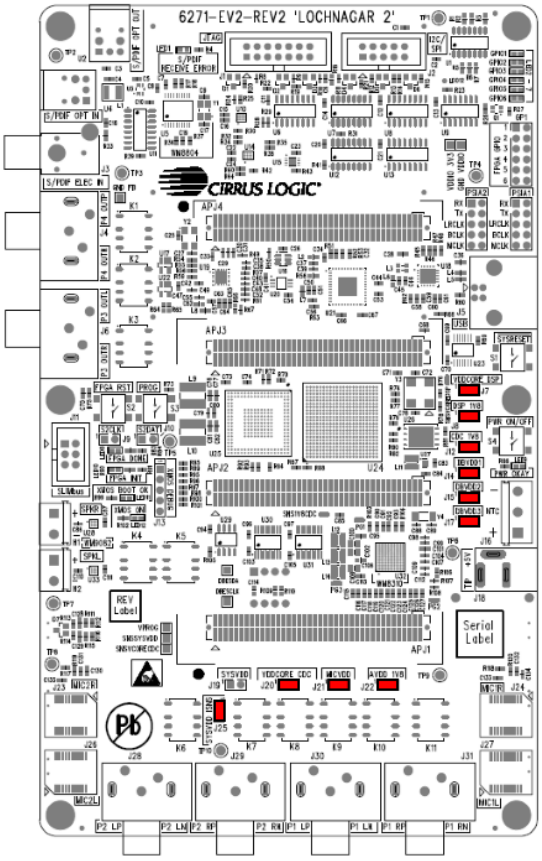
2.7.3 SLIMbus

A 2x3 box header is provided to connect Lochnagar 2 to LnK SLIMbus test systems.

2.8 Jumper Links

Lochnagar 2 has replaced most of the jumpers from the original Lochnagar board with relay switches. All analog audio routing is now controlled via the FPGA register map.

There are 11 jumpers on the Lochnagar 2 board. These are all related to power supply rails.



These jumpers allow either the isolation of certain supply rails from the minicard, or the insertion of a series ammeter between the two pins in order to measure current consumption on individual rails.

No jumper should be fitted over J19 (SYSVDD), as this will prevent the built-in current monitor circuitry from working correctly.

Header	Power Rail	Default Voltage	Jumper default
J7	VDDCORE DSP	0 V if no minicard connected 0.9 V / 1.2 V if minicard connected	On (fitted)
J8	DSP 1V8	1.8 V	On (fitted)
J12	CDC 1V8	1.8 V	On (fitted)
J14	DBVDD1	1.8 V	On (fitted)
J15	DBVDD2	1.8 V	On (fitted)
J17	DBVDD3	1.8 V	On (fitted)
J19	SYSVDD	Alternative SYSVDD jumper connection bypassing the current sense circuitry. Should only be used if the current sense circuitry is causing issues.	Off (not fitted)
J20	VDDCORE CDC	0 V if no minicard connected 0.9 V / 1.2 V if minicard connected	On (fitted)

Header	Power Rail	Default Voltage	Jumper default
J21	MICVDD	0 V default 1.8 V nominal when enabled	On (fitted)
J22	AVDD 1V8	1.8 V	On (fitted)
J25	SYSVDD ISNS	Highest of Wall, USB and battery supplies Normally 5V	On (fitted)

Note that these power rail names refer to the rails on the Lochnagar 2 board and may not directly correspond to the rails on the device/minicard. This depends entirely upon the schematic designer of the codec minicard, and how they have decided is the best method to connect the DUT to the Lochnagar system. Always refer to the board schematics if there is any doubt.

(For example, recent codec minicards such as Moon CDB47L91-M-1 do not use the DBVDD1, DBVDD2, DBVDD3, AVDD_1V8 rails, but instead derive all 1.8V rails from the single 1V8_CDC supply rail on the Lochnagar 2 and split the rails on the minicard).

3 Driver Installation and WISCE™ Support

3.1 WISCE™ Device Pack

In order to communicate with the Lochnagar 2 board, WISCE™ needs the Lochnagar 2 Device Pack to be installed.

This automatically installs the following:

- Latest version of Lochnagar 2 board firmware; use the WISCE™ configuration plugin to start the update
- Lochnagar 2 configuration plugin for WISCE™
- Current Monitor plugin for WISCE™ to monitor current on selected supply rails
- Lochnagar 2 ASIO drivers for USB audio
- Lochnagar 2 SPI/I2C communications driver
- Register map description for WISCE™
- Sample WISCE™ configuration scripts for the board

If upgrading...

It is advised to disconnect the board and close all audio streaming applications (eg. Adobe® Audition® or Foobar2000), terminal applications and JTAG debuggers before installing new versions of the Lochnagar 2 drivers. This ensures that nothing is attempting to communicate with the board during the driver installation process.

If an application is streaming audio or has an open connection to any of the drivers during the installation process, the driver installation will not be successful. The system will present itself as a "USB Composite Device" and attempts to automatically install the drivers will generate the error "This device cannot start. (Code 10)."

If this happens, the solution is to close all applications and re-install the Device Pack again from scratch.

3.2 Minimum WISCE™ Version

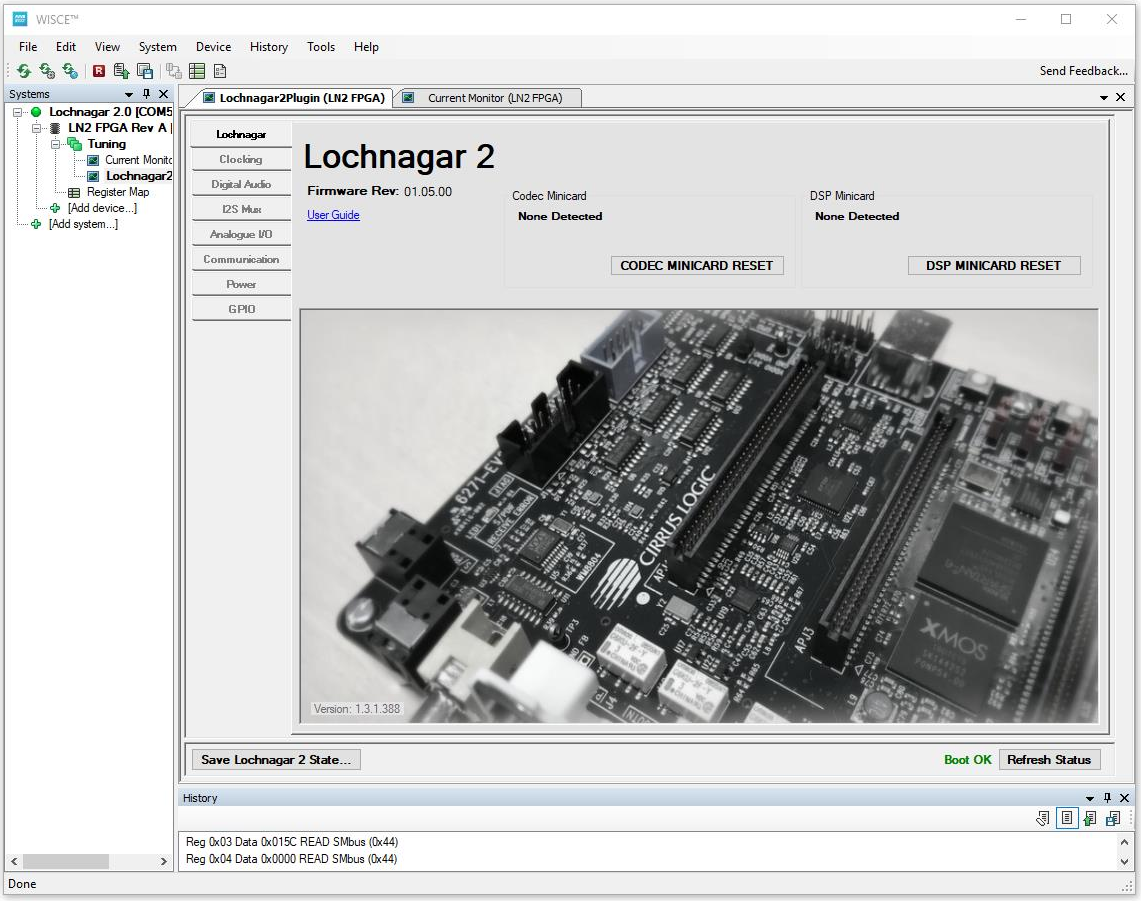
WISCE™ 3.4.0.3 provides a minimum level of support for Lochnagar 2, but does not provide the full feature set. It is strongly recommended to use version **3.5.0.21** or above.

- The current stable release of WISCE™ is available from the Cirrus Logic website: http://www.cirrus.com/en/support/software/evaluationsoftware.html

3.3 Controlling Lochnagar 2

Upon opening WISCE™, the Lochnagar 2 board should be automatically detected.

It will appear as a device called "**LN2 FPGA**" at I2C address 0x44. The **LN2 FPGA** device should have a "Tuning" folder that contains both the **Lochnagar2Plugin** and **Current Monitor** plugin. These allow for full configuration of the Lochnagar 2 board.



3.4 Lochnagar 2 Firmware Update

After installing the latest WISCE™ Device Pack (see section 3.1), restart WISCE™ and open the Lochnagar 2 Plugin.

3.4.1 Hardware Setup During Update

Firmware updates will generally work with most hardware minicards attached.

It is recommended to unplug any minicards, interposers or connectors that have their own separate power supplies during the Lochnagar 2 firmware upgrade process, as they may interfere with the process.

This includes:

- FPGA Emulation Interposers
- Zynq systems
- Amplifier minicards with separate power connections

3.4.2 Optional Update

If the Lochnagar 2 firmware is not up-to-date, a yellow box prompting the user to update the board firmware will be displayed on the main page of the plugin:

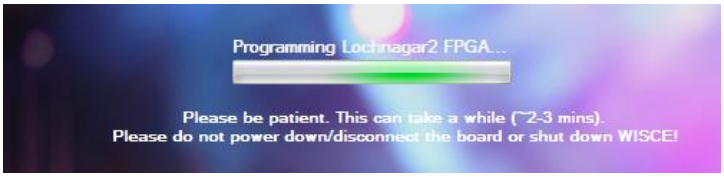
3.4.3 Forced Update

If the version of firmware on the board is so old that the plugin/register map will not function at all, the plugin will remove the element of choice and will force the user to do an update before it can operate:

> *Firmware numbers in the screenshots are for illustration purposes only and may not reflect the behaviour of actual firmware releases.*

3.4.4 Updating the Firmware

After clicking the "Update" button in the plugin, a prompt to reset the board and confirm that the user intends to do a board update is displayed. After confirming, it will take 2-3 minutes for the firmware update to complete.

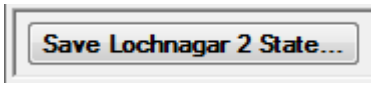


It is important not to shut down WISCE™ or power down or disconnect the Lochnagar 2 board during the firmware update process, as this may result in the Lochnagar 2 hardware becoming unusable.

3.5 Saving Lochnagar 2 Configuration to a Script

The Lochnagar 2 plugin now includes a feature that will save the full configuration of the Lochnagar 2 board as a WISCE™ text file that can be reloaded to bring the board back into exactly the same configuration. This WISCE™ profile script includes all the register sequencing required to set up the analogue paths.

To save the current configuration of the board as a WISCE™ profile script, click on the "Save Lochnagar 2 State..." button at the bottom of the plugin.



4 Boot Procedure

4.1 Boot Time

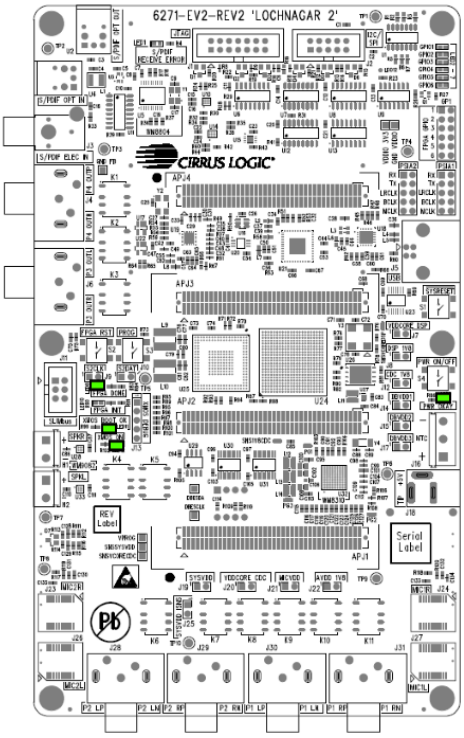
The exact boot time of Lochnagar 2 will vary depending on the version of firmware on the board, but is expected to be in the range of 2 to 5 seconds after applying power to the board. If the board is unresponsive or the SYS_STS bit still returns the "Boot in Progress" status after this time period has passed, this indicates that the boot process has failed in some way.

4.2 Board LED Configuration

After a successful boot, the following LEDs should light up in the following order:

- LED9 (PWR OKAY)
- LED8 (FPGA DONE)
- LED12 (XMOS ON)
- LED11 (XMOS BOOT OK)

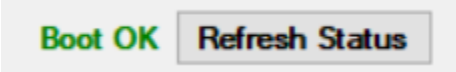
During this process the LED10 (FPGA INIT) should light up red with a quick flash, but should not remain on. The final expected LED configuration is shown below.



Any other configuration indicates that there has been an error during the boot process.

4.3 System Status Field

If any non-fatal errors happen that do not prevent communication with the board, an error code will be generated in the SYS_STS field in the R0Bh (RESET_CTRL1) register. This information is displayed in the bottom-right corner of the Lochnagar 2 Plugin along with a "Refresh Status" button that can be used to update the readback. This is the easiest way to read and interpret the system status.



The system status is always visible in the bottom-right corner of the Lochnagar 2 Plugin

From the register map view, the System Status field can be interpreted as follows. Each bit in the field has a different meaning, which allows different combinations of error messages to be present at the same time.

SYS_STS Bit	RESET_CTRL1 Bit	Meaning
0	8	0 = Boot in Progress 1 = Boot OK
1	9	1 = I2C Error
2	10	1 = ID EEPROM Error
3	11	1 = Power Config Error

4.3.1 Boot OK / Boot in Progress

This bit is set to 0 during the boot process and is only set to 1 upon successful completion. Some features of the Lochnagar 2 board (such as the analog routing features) will not operate correctly until the board has completed its boot procedure, so it is important to wait until Bit0 of the SYS_STS field returns "Boot OK" before attempting to write to other areas of the register map.

Note that the Lochnagar 2 plugin may erroneously display the "Boot in Progress" message if WISCE's cache of the register map has not been refreshed for some reason.

4.3.2 I2C Error

There was an error with the I2C bus on the device that prevented the board from booting correctly.

4.3.3 ID EEPROM Error

There was an error parsing the data on the minicard's ID EEPROM. This may lead to problems with power rail configuration or SPI chip select configuration when using the connected minicard.

It may be possible to resolve this issue by manually configuring the Lochnagar 2 register map with the correct power and/or SPI chip select configuration data.

4.3.4 Power Config Error

There was an error parsing or configuring the power rail configuration data stored on the minicard's ID EEPROM.

It may be possible to resolve this issue by manually configuring the Lochnagar 2 register map with the correct power configuration data.

5 Clocking

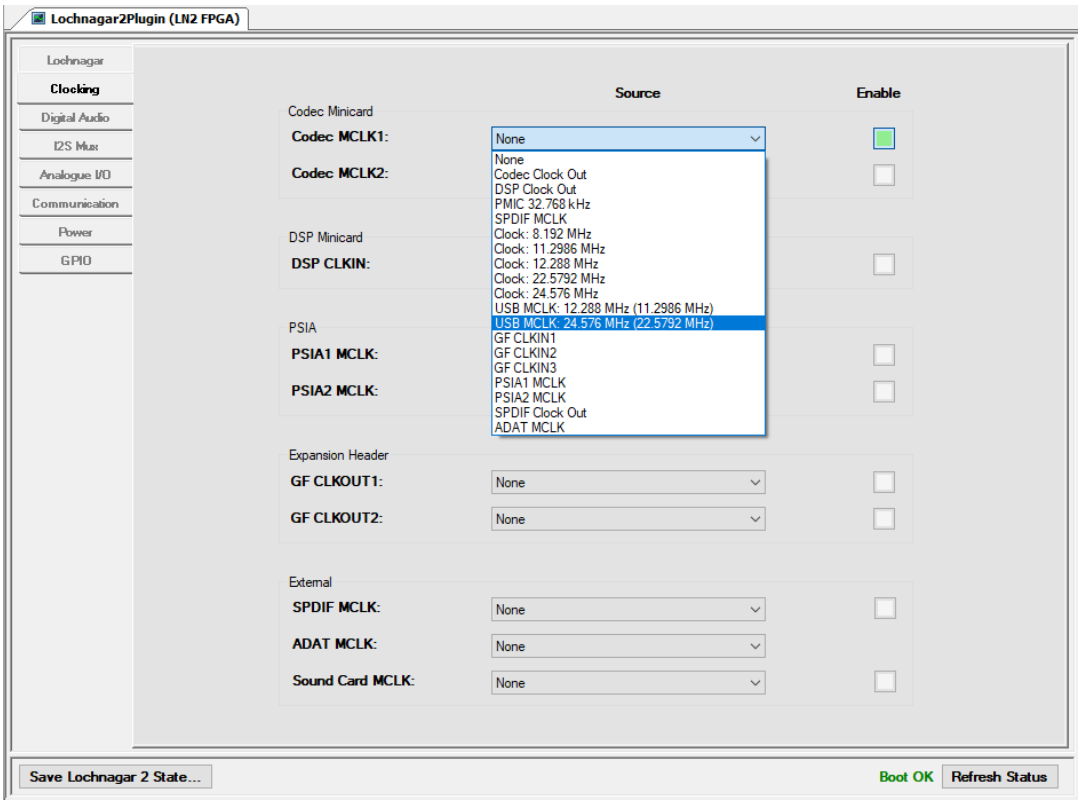
The Lochnagar 2 FPGA controls the clock routing on the board.

If no clock input is provided to the Cirrus device on the minicard, then it may not operate correctly. It is vital to configure the clocks on the Lochnagar 2 board before attempting to use the device.

5.1 Configuring Clock Routing

Digital clock signals on Lochnagar 2 are routed through the central FPGA and can connect the clock signals on the board to a number of input sources.

Routing is controlled via the **Clocking** panel of the Lochnagar 2 plugin.



5.2 Clock Setup Guide

The Lochnagar 2 FPGA manages the clocking setup of various clocks on the board.

Clock signals are separated into clock sources (available clock frequencies from a variety of sources) and clock sinks (signals that require an input clock). The Lochnagar 2 allows the user to connect any clock source to any of the available clock sinks. There are some clocks that can be either source or sink, depending on the configuration. For example, if a PSIA header is used to connect the Lochnagar 2 to an Audio Precision test system, the Audio Precision can act as either MCLK master or slave, depending on the setup. Accordingly, Lochnagar 2 allows this clock signal to be used as either a sink or a source.

Lochnagar 2 has an on-board clock generator that generates the following frequencies: 11.2986 MHz, 12.288 MHz, 22.5792 MHz and 24.576 MHz. In addition, clocks can be provided from the USB streaming peripheral, PSIA headers, GF Expansion Headers, PMIC chip, clock output pins from the codec or DSP minicards, the S/PDIF transceiver or ADAT source.

When using digital audio with Cirrus Logic Smart Codec devices, the MCLK signal provided to the chip should be synchronous with any digital audio interfaces used on the chip. For example, if using the audio from the USB audio streaming, the MCLK provided to the slave device needs to be synchronous with the audio data coming from the USB audio streamer. For this reason, USB, PSIA, S/PDIF and ADAT MCLK signals are provided as available clock sources in the **Clocking** panel.

5.2.1 Example Configuration

To connect the USB MCLK signal to the Sound Card clock:

1. Open the **Clocking** panel of the plugin
2. Find the row associated with the Sound Card MCLK clock sink
3. Select USB MCLK: 24.576 MHZ (22.5792 MHz) Clock Source from the drop-down menu on the Sound Card MCLK row.
4. Click the enable button on the same row

This will provide the 24/22 MHz USB MCLK signal into the Sound Card peripheral.

5.3 Descriptions of Clock Sinks and Sources

5.3.1 List of Clock Sinks

The following table lists all the potential destinations that clock signals can be routed to on Lochnagar 2. The register map addresses for the control registers associated with these clock sinks are provided for advanced users.

Clock Sink	Control Register	Description
Codec MCLK1	R1Eh	Master clock input on the codec minicard
Codec MCLK2	R1Fh	Master clock input on the codec minicard
DSP CLKIN	R20h	Clock input on the DSP minicard
PSIA1 MCLK	R21h	Master clock input or output signal on the PSIA1 pin headers
PSIA2 MCLK	R22h	Master clock input or output signal on the PSIA2 pin headers
GF CLKOUT1	R24h	Clock output to the GF expansion headers
GF CLKOUT2	R25h	Clock output to the GF expansion headers
SPDIF MCLK	R23h	Master clock input or output signal for the S/PDIF interface
ADAT MCLK	R26h	Master clock input or output signal for the ADAT interface
Sound Card MCLK	R27h	Clock input signal to the Sound Card hardware on underside of Lochnagar 2

5.3.2 List of Clock Sources

The following table lists all the potential sources of clock signals that can be routed to the clock sinks listed in the table above. The binary values for these sources are provided for advanced users.

Clock Source	Binary Value	Description
None	0x00	No clock source selected
Codec Clock Out	0x01	Clock output signal generated by the codec
DSP Clock Out	0x02	Clock output signal generated on the DSP minicard
PMIC 32.768 kHz	0x03	32.768 kHz clock generated by the onboard power management IC
SPDIF MCLK	0x04	Use this clock input for S/PDIF audio use cases Clock output from the S/PDIF receiver chip. Frequency will depend upon sampling rate of SP/DIF audio. With no S/PDIF signal applied, the chip generates a default of 12.0 MHz
Clock: 8.192 MHz	0x09	Fixed 8.192 MHz (16k multiple) clock from onboard clock generator chip.
Clock: 12.288 MHz	0x05	Fixed 12.288 MHz (48k multiple) clock from onboard clock generator chip.
Clock: 11.2986 MHz	0x06	Fixed 11.2986 MHz (44.1k multiple) clock from onboard clock generator chip.

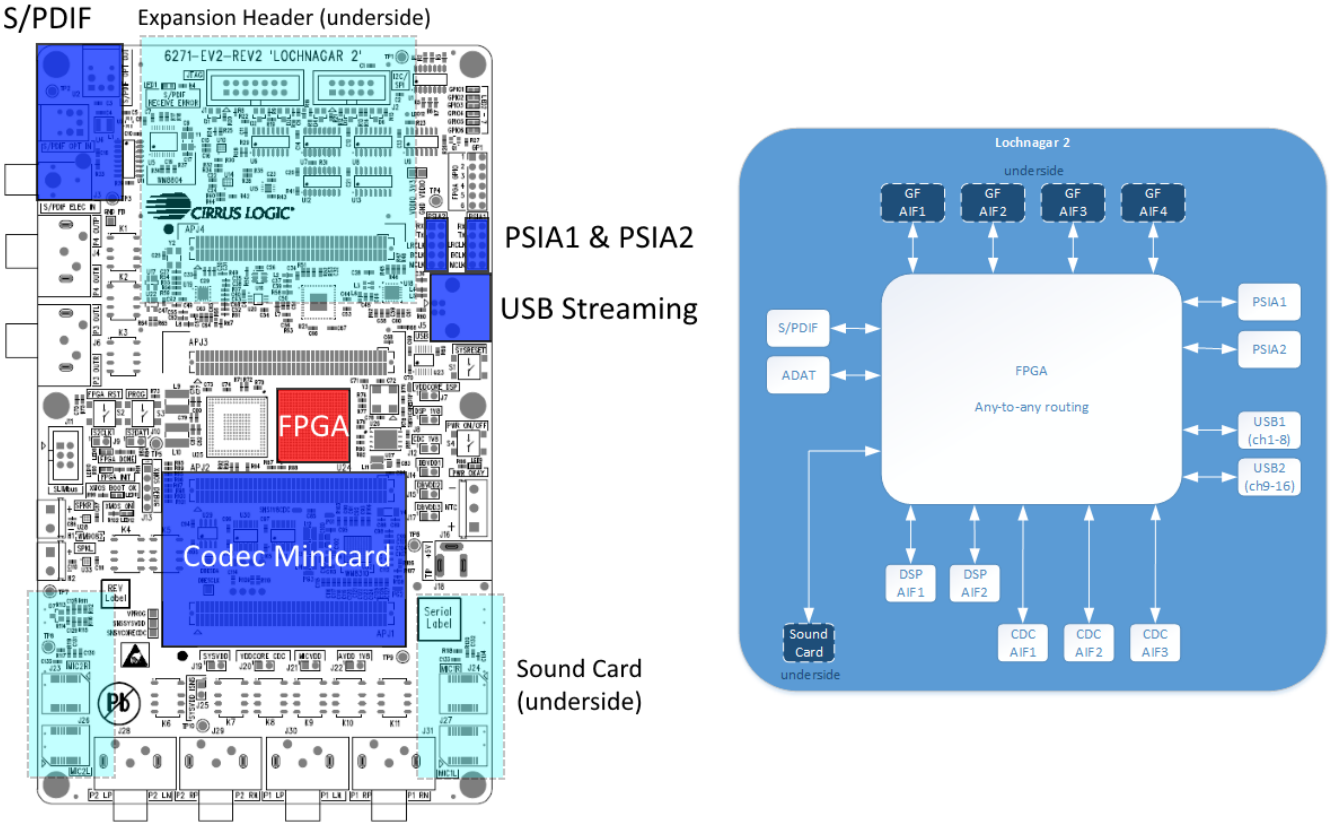
Clock Source	Binary Value	Description
Clock: 24.576 MHz	0x07	Fixed 24.576 MHz (48k multiple) clock from onboard clock generator chip.
Clock: 22.5792 MHz	0x08	Fixed 22.5792 MHz (44.1k multiple) clock from onboard clock generator chip.
USB MCLK: 12.288 MHz (11.2986 MHz)	0x12	Use this clock input for USB streaming use cases Half rate clock that is synchronous to USB audio data. Frequency will depend on the sampling rate of audio being transferred over USB This will be either 12.288 MHz or 11.2986 MHz
USB MCLK: 24.576 MHz (22.5792 MHz)	0x0A	Use this clock input for USB streaming use cases Full rate clock that is synchronous to USB audio data. Frequency will depend on the sampling rate of audio being transferred over USB This will be either 24.576 MHz or 22.5792 MHz
GF MCLK1	0x0B	Clock signal from the expansion headers on underside. Usually used when connected to Linux Application Processor systems
GF MCLK2	0x0D	Clock signal from the expansion headers on underside. Usually used when connected to Linux Application Processor systems
GF MCLK3	0x0C	Clock signal from the expansion headers on underside. Usually used when connected to Linux Application Processor systems
PSIA1 MCLK	0x0E	Clock signal applied to PSIA1 headers (3.3V I2S pin headers)
PSIA2 MCLK	0x0F	Clock signal applied to PSIA2 headers (3.3V I2S pin headers)
SPDIF Clockout	0x10	Secondary clock output signal from the S/PDIF receiver chip. For advanced use cases only.
ADAT MCLK	0x11	Clock signal from the ADAT receiver when used in ADAT mode.
(ADAT MCLK Only) External ADAT Clock	n/a	This option in the drop-down menu does not set a value to ADAT_MCLK_SRC, but instead enables the ADAT_MCLK_ENA bit in the register map. This bit behaves differently for ADAT MCLK compared to the other clocks. When set, this mode uses a PLL to recover the incoming ADAT master clock from the optical cable. If any other value is selected in the drop-down, the ADAT_MCLK_ENA bit is unset and the source specified in ADAT_MCLK_SRC is used for the ADAT MCLK signal.

6 Digital Audio

This section details the digital audio inputs and outputs on the Lochnagar 2 board, and how to configure the routing. Any digital audio interface (AIF) on the Lochnagar 2 system can be connected to any other via the flexible routing of the FPGA.

6.1 Digital Audio Connection Diagrams

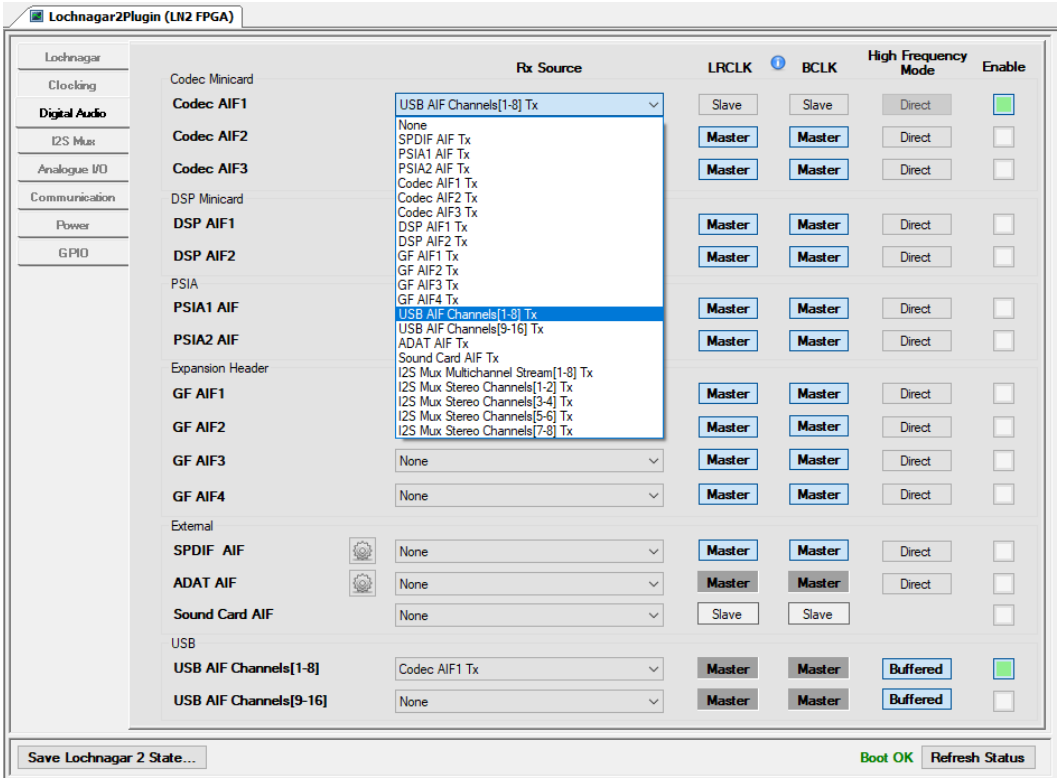
The following diagram details the digital audio inputs and outputs on the Lochnagar 2 board.



6.2 Configuring Digital Audio Routing

Digital audio signals on Lochnagar 2 are routed through the central FPGA and can connect any AIF port to any other AIF port on the board.

Routing is controlled via the **Digital Audio** panel of the Lochnagar 2 plugin.



6.2.1 BCLK/LRCLK Routing Operation

The **Rx Source** drop-down menu selects where the audio data comes from for the AIF sink on that row.

- If **BCLK/LRCLK** are set to **Slave**, the Lochnagar 2 board will supply the clocks from the audio interface selected in the **Rx Source** selection.
- If **BCLK/LRCLK** are set to **Master**, the Lochnagar 2 will not provide any clocks outputs to the AIF sink. The pins will be put into high-Z mode and used as inputs.

Clocks in Slave Mode

If BCLK and/or LRCLK for an AIF device are set to "Slave" mode, the Rx Source should not be set to "None", as this will mean that no clocks are provided to the AIF Slave device.

6.2.2 High Frequency Mode

Path delays in Digital Audio systems can cause problems when the round trip delay between the Digital Audio master and slave devices is comparable to the period of the bit clock. In these scenarios, the return data received by the master may be corrupted. Lochnagar 2 provides a buffered "High Frequency Mode" setting that will compensate for long round trip delays by introducing a single audio frame of buffering into the AIF master return data.

System level propagation delays must be taken into account.

High Frequency Mode is required when the Digital Audio bit clock is higher than 6.144 MHz and should allow correct operation for bit clocks up to 24.576 MHz in ideal operating conditions. As USB streaming on Lochnagar 2 is multi-channel, it uses relatively high bit clock rates, so it is therefore recommended to set the High Frequency Mode to "Buffered" for all sampling rates above 24 kHz when using the USB streaming feature. The frequencies quoted are guidelines for ideal operating conditions, but several external factors on the PCB itself may add extra round trip delay. If margins are exceeded by external factors, High Frequency Mode may need to be enabled at a lower frequency than expected or may not be able to compensate at all. These external delay factors include high bus capacitance, large clock

to data propagation delays (> 15 ns) on the slave device, or minicards that have long PCB tracks or cabling.

The High Frequency Mode setting is only available on AIF peripherals where both BCLK and LRCLK are configured as AIF master.

There are two potential settings:

- Direct Mode = No buffering or delay is added onto this AIF signal by the Lochnagar 2 board
- Buffered Mode = A single audio frame of delay is introduced to the data received by this AIF master from the Rx Source.

Direct Mode is the default setting as it provides the lowest possible latency through the system. If audio corruption is observed at the AIF master, it is possible to resolve this by enabling the "Buffered" High Frequency Mode setting.

6.2.3 Example Configuration

To set up an AIF connection between the USB audio streaming and Codec AIF1 port:

1. Find the Codec AIF1 row on the **Digital Audio** tab of the Lochnagar 2 plugin.
2. Select an Rx Source for this audio connection. Choose USB AIF Channels[1-8] Tx to connect it to the USB streaming peripheral.
3. Select whether Codec AIF1 is master or slave for the BCLK and LRCLK. Since USB streaming operates as master only, they must both be set to Slave in this example.
4. If audio is required in both directions, find the row for USB AIF Channels[1-8], and set the Rx Source to Codec AIF1 Tx. This will make the audio bidirectional.
5. If required, select the Buffered High Frequency Mode on the USB AIF Channels[1-8] row to add optional buffering into the return path. This may be required if the return data from the codec is corrupted due to path length delays.
6. Enable both interfaces using the buttons on the right of each row.

It is also important to make sure that the codec has an MCLK that is connected to a synchronous clock source. In this scenario, the **Clocking** panel of the plugin should be used to set MCLK1 or MCLK2 to the USB MCLK.

6.2.4 Advanced Clocking Configurations

Audio paths do not need to be set up directly between two AIF interfaces, and BCLK/LRCLK do not necessarily have to be driven by the same master or in the same direction, assuming that the Slave device also supports that mode. A single AIF master could potentially clock multiple slave devices by daisy-chaining the audio from one slave AIF port to the next.

This flexibility means that the Lochnagar 2 can be set up to emulate almost any potential AIF configuration in order to develop solutions or replicate problems.

Note that there is no protection for scenarios where the FPGA is configured incorrectly, so it is also important to make sure that the AIF interface connected to the FPGA is configured in the appropriate manner. If Codec AIF1 is set up as a Master on the Cirrus Logic Smart Codec device and also in the FPGA, the two devices will drive against each other on the line and potentially create mid-rail voltages.

6.3 AIF Interfaces on Codec Minicard

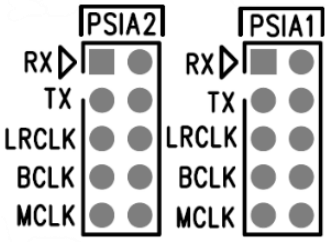
The codec minicard supports up to three AIF interfaces (for smaller cards with two connectors) or five AIF interfaces (for larger cards that span over three connectors).

6.4 AIF Interfaces on the Expansion Headers

The expansion headers on the underside of Lochnagar 2 are designed to connect Lochnagar 2 to Linux Application Processor systems. The headers on the underside support up to four AIF interfaces.

6.5 PSIA Headers

The PSIA headers are designed to connect to Audio Precision testing equipment through the PSIA (Programmable Serial Interface Adapter) hardware.



This is essentially a standard I2S-based digital audio interface with 3.3V signal levels, consisting of the following signals:

- RXDAT (pin 1)
- TXDAT (pin 3)
- LRCLK (pin 5)
- BCLK (pin 7)
- MCLK (pin 9)
- Ground signals (pins 2, 4, 6, 8, 10)

The silkscreen markings on Lochnagar 2 will help the user determine which pin is which. Note that TX and RX directions are with respect to the external PSIA hardware, therefore the pin marked "RX" is an output from the FPGA.

Clocking

When using the PSIA with a Cirrus codec device, the codec can be used as either AIF clock master or clock slave. The **Clocking** panel of the Lochnagar 2 Plugin should be used to configure the MCLKs of the codec and PSIA ports appropriately.

6.6 S/PDIF and ADAT

There are S/PDIF optical and electrical input connectors on Lochnagar 2, and a single S/PDIF optical output connector. Lochnagar 2 also supports using ADAT protocol with the optical connectors.

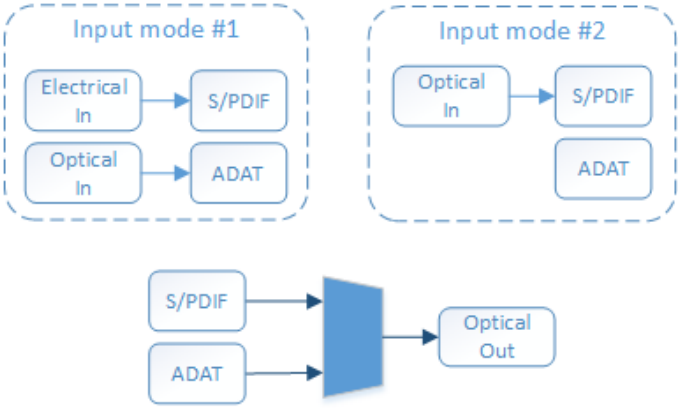
ADAT

Lochnagar 2 only supports ADAT protocol with 48 kHz sampling rate, and it can only be used in I2S clock master mode.

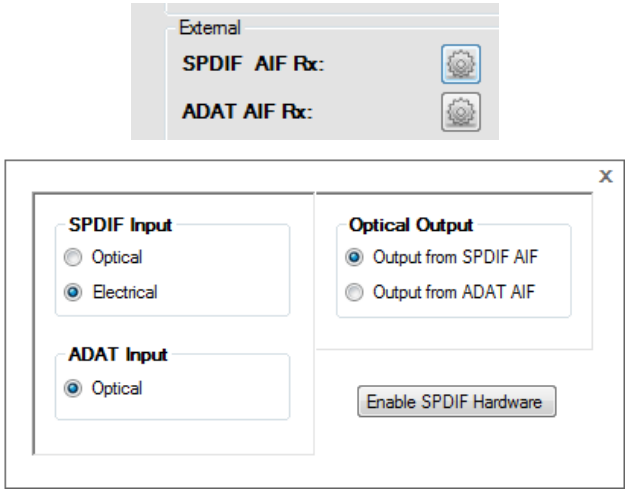
6.6.1 Standard Use Cases

- S/PDIF can be used with either electrical or optical input connector.
- ADAT can only be used with the optical input. If the optical input is already being used for S/PDIF, it cannot be used for ADAT.

There is only a single optical output, and can be used with either the S/PDIF or ADAT output.



These configuration options can be selected within the **Digital Audio** panel of the Lochnagar 2 Plugin. Click the cogwheel-shaped "setup" icon next to either "SPDIF AIF Rx" or "ADAT AIF Rx" to bring up the S/PDIF and ADAT configuration options panel.



If using S/PDIF, it is important to click the "Enable SPDIF Hardware" button on this panel to bring the WM8804 S/PDIF transceiver chip out of reset.

Clocking

When using S/PDIF or ADAT audio as clock masters with a Cirrus Logic codec device in slave mode, it is important that one of the codec's MCLK pins is connected to a clock source that is synchronous to the audio coming from the S/PDIF or ADAT source.
The **Clocking** panel of the Lochnagar 2 Plugin should be used to assign either MCLK1 or MCLK2 to one of the SPDIF MCLK or ADAT MCLK sources as appropriate.

6.6.2 Advanced Use Cases

Lochnagar 2 also supports more advanced use case configurations using the WM8804 S/PDIF transceiver chip, including operating in clock slave mode. Since these require the additional configuration of the WM8804 chip, these modes cannot be enabled through the Lochnagar 2 plugin and are left for advanced users only.

Firstly, the I2C bridge to the WM8804 chip must be enabled. This will connect the primary I2C bus on the system (I2C1) to the SPDIF I2C bus (SPDIF_I2C):

SPDIF_I2C_BRIDGE1_ENA	I2C4_BRIDGE1_ENA	I2C3_BRIDGE1_ENA	I2C2_BRIDGE1_ENA	I2C1_BRIDGE1_ENA
1	0	0	0	1

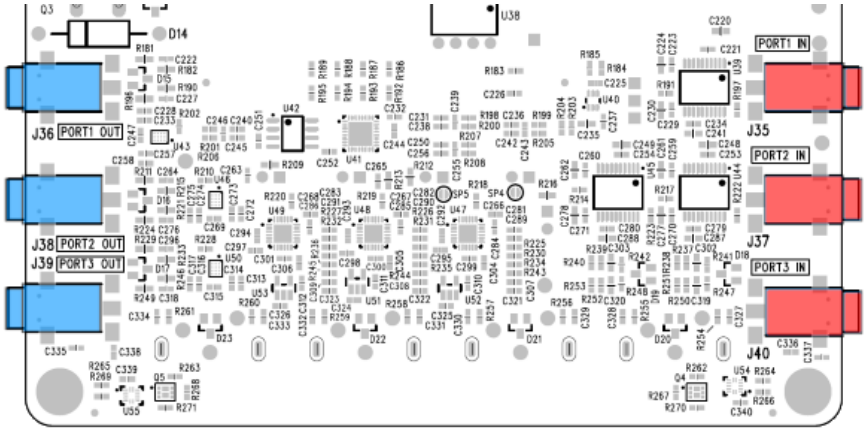
The WM8804 should be placed into Software Control mode (SPDIF_HWMODE = 0) and then taken out of reset (SPDIF_RESET_N = 1):

SPDIF_HWMODE	SPDIF_IN_SEL	SPDIF_TX_SEL	SPDIF_RESET_N
0	1	0	1

The WM8804 control interface can now be accessed over I2C and configured into a custom mode.

6.7 Sound Card

There are 3 x stereo input 3.5 mm jacks and 3 x stereo output 3.5 mm jacks on the underside of Lochnagar 2. These comprise the "Sound Card".



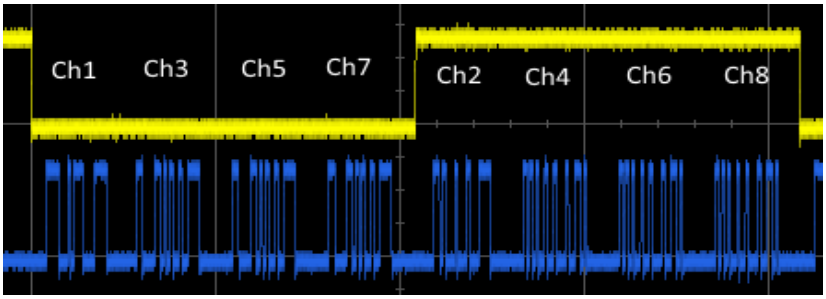
3.5 mm Jacks on underside of Lochnagar 2. Output Ports in Blue, Input Ports in Red

These inputs and outputs are not connected directly to analog ports on the minicard, but are presented as digital audio I/O within the **Digital Audio** routing panel of the Lochnagar 2 Plugin. Audio from any AIF port on the Lochnagar can be routed directly to the Sound Card.

6.7.1 Sound Card Audio Format

- The Sound Card expects to receive a 4- or 8-channel Multichannel I2S signal. This means the BCLK must be either 128 or 256 times the LRCLK rate (128Fs or 256Fs). If using 128Fs, channels 5 and 6 will not be available.
- Each sample should be supplied in a 32-bit wide slot, regardless of the audio word length. When 16- or 24-bit audio samples are used, zero-padding must follow so that 32-bits are used per sample.
- The Sound Card will always be the BCLK/LRCLK slave
- The Sound Card must be provided with a synchronous MCLK in the **Clocking** panel of the Lochnagar 2 Plugin.

The Sound Card requires the same multichannel I2S format as that generated by the USB streaming module.



The channels in the I2S stream will map directly to the 3.5 mm jacks as shown below.

PORT1 left	1
PORT1 right	2
PORT2 left	3
PORT2 right	4
PORT3 left	5
PORT3 right	6

This channel mapping applies to both input and output ports. The data on channels 7 and 8 is discarded on the output side and zero-filled (silence) on the input side.

6.7.2 Enabling the Sound Card

The Sound Card is enabled within WISCE™ as follows:

1. Set up a clock source for the Sound Card MCLK on the **Clocking** panel and enable it
2. Set up the Sound Card as a source or sink within the **Digital Audio** panel
3. Click the enable button on the Sound Card row

Clocking

The Sound Card always operates in clock slave mode. An Rx Source must be selected in order to supply BCLK and LRCLK signals.

In addition, the **Clocking** panel of the Lochnagar 2 Plugin should be used to assign an appropriate clock source to the Sound Card MCLK input. Without a synchronous MCLK input, the Sound Card will not function correctly.

6.8 Descriptions of Digital Audio Sinks and Sources

6.8.1 List of Digital Audio Sinks

The table below lists all the potential destinations that digital audio signals can be routed to on Lochnagar 2. The register map addresses for the control registers associated with these AIF sinks are provided for advanced users.

Category	Name	Control Register	Description
Codec Minicard	Codec AIF1	R0Dh	AIF1 port on the codec minicard
Codec Minicard	Codec AIF2	R0Eh	AIF2 port on the codec minicard
Codec Minicard	Codec AIF3	R0Fh	AIF3 port on the codec minicard
DSP / Codec Minicard	DSP AIF1 / Codec AIF4	R10h	How this interface is displayed in the plugin will depend upon your minicard May be either AIF4 on codec minicard or AIF1 on DSP minicard (obsolete)

Category	Name	Control Register	Description
DSP / Codec Minicard	DSP AIF2 / Codec AIF5	R11h	How this interface is displayed in the plugin will depend upon your minicard May be either AIF5 on codec minicard or AIF2 on DSP minicard (obsolete)
PSIA	PSIA1 AIF	R12h	PSIA pin headers for connection to Audio Precision PSIA or debug
PSIA	PSIA2 AIF	R13h	PSIA pin headers for connection to Audio Precision PSIA or debug
Expansion Header	GF AIF1	R16h	Expansion header on underside of Lochnagar 2
Expansion Header	GF AIF2	R17h	Expansion header on underside of Lochnagar 2
Expansion Header	GF AIF3	R14h	Expansion header on underside of Lochnagar 2
Expansion Header	GF AIF4	R15h	Expansion header on underside of Lochnagar 2
External	SPDIF AIF	R18h	S/PDIF optical input/output *Note: Basic use case is clock master only.* *If S/PDIF is used in clock slave mode, it will require extra configuration on the WM8804 S/PDIF transceiver chip to operate correctly.* *Note: S/PDIF requires extra configuration before it will operate.* *Click on the cogwheel 'setup' icon to select ADAT / S/PDIF options.*
External	ADAT AIF	R1Bh	ADAT optical input/output *Note: ADAT can be used in clock master mode only. If ADAT is in use, then S/PDIF will be limited to electrical input only.* *Note: ADAT requires extra configuration before it will operate.* *Click on the cogwheel 'setup' icon to select ADAT / SP/DIF options.*
External	Sound Card AIF	R180h	Analog audio inputs and outputs through the 3.5 mm jacks on underside of the board. A clock supply must also be provided to the Sound Card before it will operate.
USB	USB AIF Channels[1-8]	R19h	USB audio streaming ASIO channels 1-8 *Note: USB streaming can only function in clock master mode*
USB	USB AIF Channels[9-16]	R1Ah	USB audio streaming ASIO channels 9-16 *Note: USB streaming can only function in clock master mode*
I2S Mux	I2S Mux Multichannel Stream[1-8] Rx	R181h	8 channel I2S stream to the I2S Mux Converter block *Note: This control is located on the I2S Mux Panel of the Lochnagar2Plugin*
I2S Mux	I2S Mux Stereo Channels[1-2] Rx	R182h	Channels 1-2 to the stereo to 8-channel conversion in the I2S Mux Converter block *Note: This control is located on the I2S Mux Panel of the Lochnagar2Plugin*
I2S Mux	I2S Mux Stereo Channels[3-4] Rx	R183h	Channels 3-4 to the stereo to 8-channel conversion in the I2S Mux Converter block *Note: This control is located on the I2S Mux Panel of the Lochnagar2Plugin*
I2S Mux	I2S Mux Stereo Channels[5-6] Rx	R184h	Channels 5-6 to the stereo to 8-channel conversion in the I2S Mux Converter block *Note: This control is located on the I2S Mux Panel of the Lochnagar2Plugin*
I2S Mux	I2S Mux Stereo Channels[7-8] Rx	R185h	Channels 7-8 to the stereo to 8-channel conversion in the I2S Mux Converter block *Note: This control is located on the I2S Mux Panel of the Lochnagar2Plugin*

6.8.2 List of Digital Audio Sources

The table below lists all the potential sources of digital audio data that can be routed to the Digital Audio sinks listed in the table above. The binary values for these sources are provided for advanced users.

Category	Name	Binary Value	Description
	None	0x00	No audio source connected to this sink
External	SPDIF AIF Tx	0x01	S/PDIF optical or electrical input
PSIA	PSIA1 AIF Tx	0x02	PSIA pin headers for connection to Audio Precision PSIA or debug
PSIA	PSIA2 AIF Tx	0x03	PSIA pin headers for connection to Audio Precision PSIA or debug
Audio Card	Codec AIF1 Tx	0x04	AIF1 port on the codec minicard
Audio Card	Codec AIF2 Tx	0x05	AIF2 port on the codec minicard
Audio Card	Codec AIF3 Tx	0x06	AIF3 port on the codec minicard
DSP Card / Audio Card	DSP AIF1 Tx / Codec AIF4 Tx	0x07	How this interface is displayed in the plugin will depend upon your minicard May be either AIF4 on codec minicard or AIF1 on DSP minicard (obsolete)

Category	Name	Binary Value	Description
DSP Card / Audio Card	DSP AIF2 Tx / Codec AIF5 Tx	0x08	How this interface is displayed in the plugin will depend upon your minicard May be either AIF5 on codec minicard or AIF2 on DSP minicard (obsolete)
Expansion Header	GF AIF1 Tx	0x0B	Expansion header on underside of Lochnagar 2
Expansion Header	GF AIF2 Tx	0x0C	Expansion header on underside of Lochnagar 2
Expansion Header	GF AIF3 Tx	0x09	Expansion header on underside of Lochnagar 2
Expansion Header	GF AIF4 Tx	0x0A	Expansion header on underside of Lochnagar 2
USB	USB AIF Channels[1-8] Tx	0x0D	USB audio streaming input (from PC) ASIO channels 1-8 *Note: USB streaming can only function as clock master*
USB	USB AIF Channels[9-16] Tx	0x0E	USB audio streaming input (from PC) ASIO channels 9-16 *Note: USB streaming can only function as clock master*
External	ADAT AIF Tx	0x0F	ADAT optical input. *Note: the ADAT hardware will need additional configuration* *Click the cogwheel Setup icon to complete ADAT setup*
External	Sound Card AIF Tx	0x10	Analog inputs from the 3.5 mm jacks on the underside of Lochnagar 2 *Note: an MCLK for the Sound Card must be configured in the clocking panel* For more details, see: Sound Card
I2S Mux	I2S Mux Multichannel Stream[1-8] Tx	0x11	8 channel I2S stream from the I2S Mux block *Note: See I2S Mux panel to complete the setup*
I2S Mux	I2S Mux Stereo Channels[1-2] Tx	0x12	De-muxed channels 1-2 from the 8-channel TDM to stereo I2S conversion in the I2S Mux block *Note: See I2S Mux panel to complete the setup*
I2S Mux	I2S Mux Stereo Channels[3-4] Tx	0x13	De-muxed channels 3-4 from the 8-channel I2S to stereo I2S conversion in the I2S Mux block *Note: See I2S Mux panel to complete the setup*
I2S Mux	I2S Mux Stereo Channels[5-6] Tx	0x14	De-muxed channels 5-6 from the 8-channel I2S to stereo I2S conversion in the I2S Mux block *Note: See I2S Mux panel to complete the setup*
I2S Mux	I2S Mux Stereo Channels[7-8] Tx	0x15	De-muxed channels 7-8 from the 8-channel I2S to stereo I2S conversion in the I2S Mux block *Note: See I2S Mux panel to complete the setup*

7 USB Audio Streaming

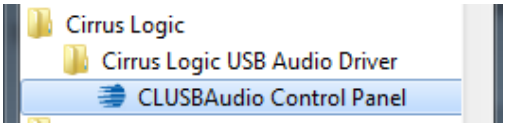
The Lochnagar 2 board presents itself as a USB audio device to the host PC using USB Audio Class 2 to transfer audio data.

Do not reset or power down when streaming USB audio

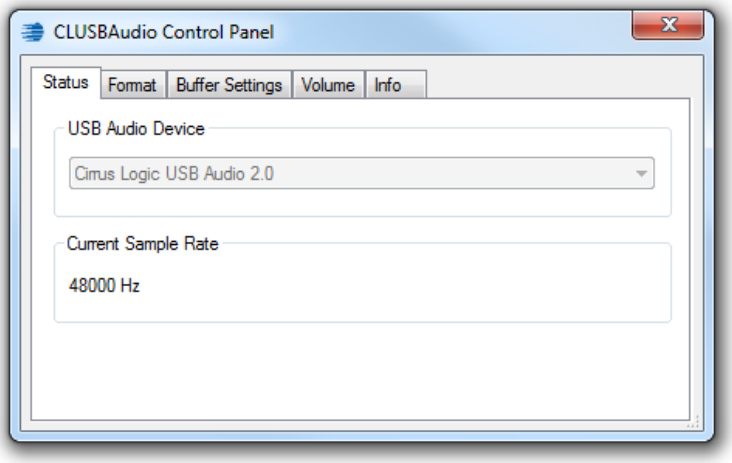
If the Lochnagar 2 board is streaming USB Audio 2.0 when it is reset, the Windows audio drivers will stall. This is a common issue with Windows audio drivers when using external USB sound cards. When Lochnagar 2 is reconnected to the system, it may then fail to connect to WISCE due to the audio driver issues. In order to reconnect, the application playing USB audio to the Lochnagar 2 board must be stopped. If a failed attempt at connecting to WISCE™ has already occurred, the Lochnagar 2 board may need another reset in order to re-establish communications with the system.

7.1 CLUSBAudio Control Panel

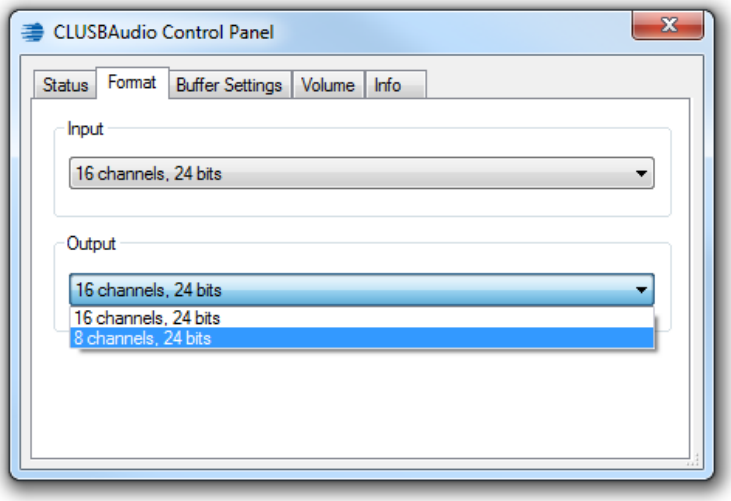
The CLUSBAudio Control Panel is for the Lochnagar 2 USB audio streaming system. A link to the panel can be found in the "Cirrus Logic" folder in the Start Menu.



The main **Status** tab of the CLUSBAudio Control Panel will display the Current Sampling Rate being used by Lochnagar 2. This is determined by either the Windows drivers setting (for DirectSound) or the audio software (for example Adobe Audition) for ASIO or WASAPI. This is useful for confirmation that audio is playing at the correct sampling rate.



The **Format** tab may be required for use cases where the sampling rate is 192 or 176.4 kHz. Due to limitations in bandwidth, Lochnagar 2 cannot support a full 16 channels of 24-bit audio at these sample rates, so the channel count must be reduced to 8 channels. On this tab, 'Input' refers to audio coming from Lochnagar 2 into the PC, and 'Output' refers to audio being transferred from the PC to Lochnagar 2.



For all other sampling rates:

- 16 channels, 24 bits (**default recommended option**)

For 192 kHz or 176.4 kHz:

- 8 channels, 24 bits

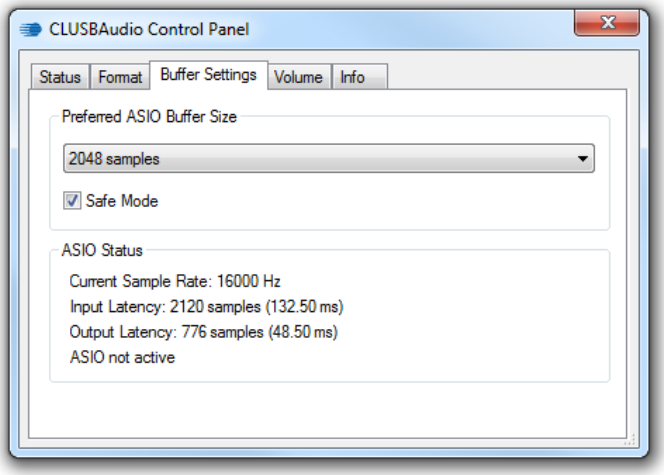
The format of the Input channels should match that of the Output channels.

For all use cases other than 192 kHz or 176.4 kHz sampling rates, it is recommended to keep these settings at the default value of 16 channels at 24 bits. Note that the input and output format selection made here will apply to the audio streaming device regardless of the audio drivers used (ASIO, WASAPI, DirectSound) so it is important to make sure this selection is correct if 192 kHz audio is to be played.

192 kHz Mode

For 192 kHz and 176.4 kHz sampling rates, only the 8 channels / 24 bit mode will operate correctly. If 16 channels is used for either input or output, it will create bit-shifts (and therefore audible distortion) when WISCE™ is used at the same time as audio streaming. Both Input and Output settings must be set to 8 channel/24-bit mode in the CLUSBAudio Control panel. This is true regardless of whether you are using Windows DirectSound, WASAPI or ASIO drivers.

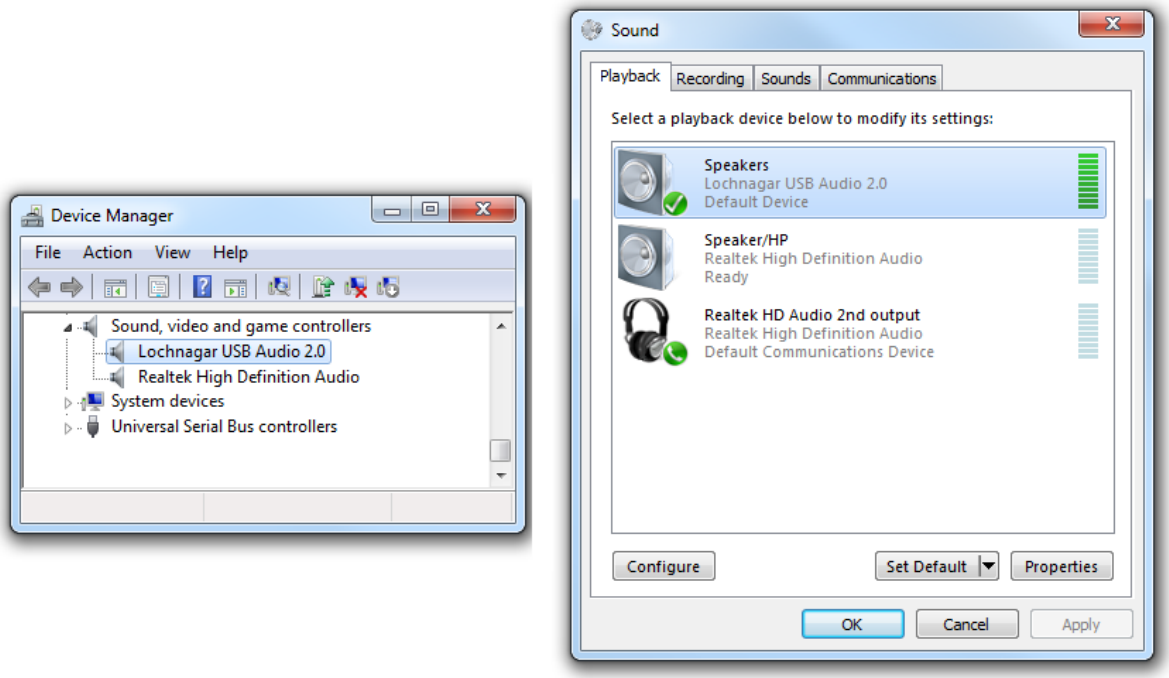
The **Buffer Settings** tab settings can be modified to provide a larger or smaller USB buffer, but be aware that some applications (e.g. Adobe Audition) may have problems with particular combinations of sample rate and buffer size. The "safe mode" setting provides extra tolerance for ASIO audio applications if they are not able to keep up with the audio demand at the expense of a slightly increased latency. It is recommended to keep this option enabled.



7.2 Using Lochnagar 2 with Windows WDM

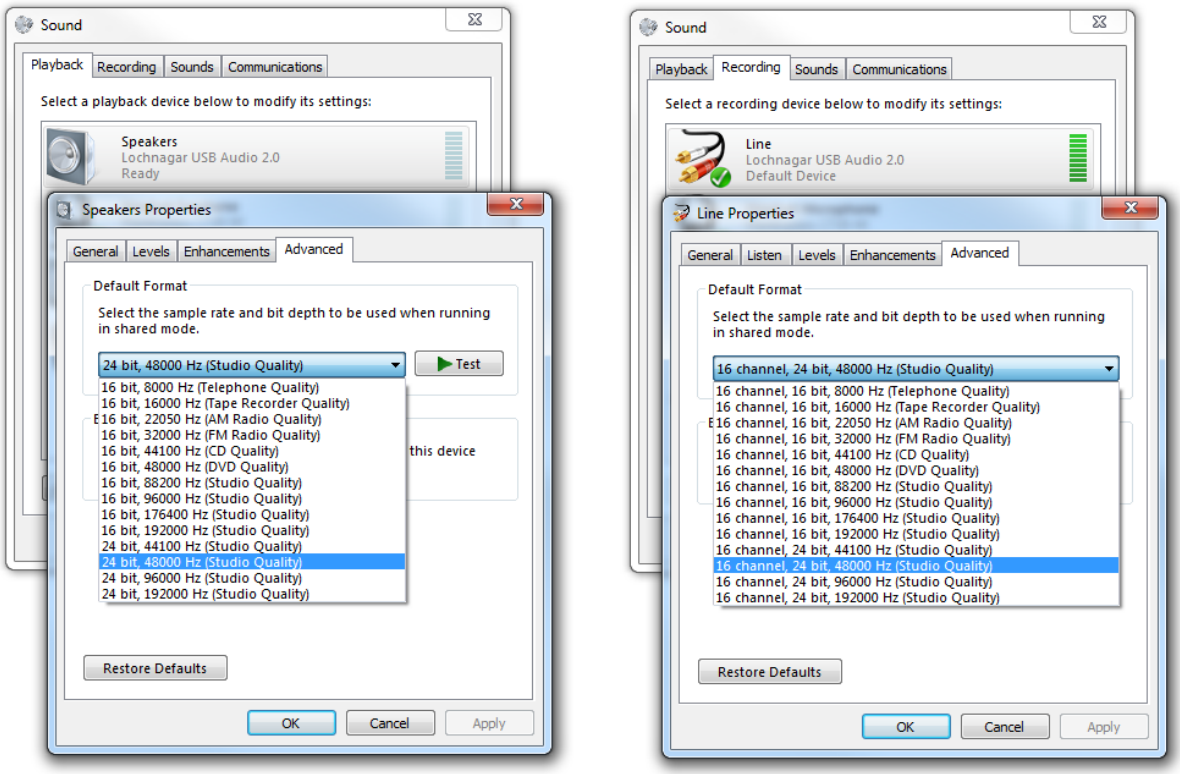
Lochnagar 2 can act and function as a normal stereo USB audio device on a Windows system using Windows WDM drivers. Although Windows Vista introduced native support for WASAPI, which is technically superior, WDM is still the default audio driver for all Windows OS versions.

Stereo audio from standard Windows applications (Media Player, iTunes®, Spotify®, web browsers) can be routed through the Lochnagar 2 by simply selecting it as the default audio device on the system within the Control Panel.



This has some limitations. Firstly, it only supports 2 channels, and all audio will be resampled by Windows to the sampling rate set within the Advanced panels of the "Speakers Properties" display (accessed by right-clicking on 'Speakers/Lochnagar USB Audio 2.0' in the window shown above). The input channels will operate at the rate set within the Advanced panel of the "Line Properties" display.

If the USB audio streaming is used for simultaneous playback and recording, the playback and record sampling rates must be set to the same value. It is also important to ensure that the format for the recording device matches the configuration of the CLUSBAudio panel in terms of number of channels and bit depth.



7.3 Using Lochnagar 2 with WASAPI

With Windows Vista, Microsoft introduced the Windows Audio Session Application Programming Interface (WASAPI) audio transport method. This is technically superior to WDM and offers lower distortion and options to bypass mixing if used in Exclusive mode, similar to ASIO default functionality. It allows the user to set the audio sampling rate through the application, rather than the Control Panel audio device properties, allowing for easier support for multiple sampling rates.

Note that although WASAPI itself is included with Windows, most standard applications do not use it and even media players such as Foobar require an extra WASAPI plugin to interface with the transport. The WASAPI interface to Lochnagar 2 will appear in the media player's device selection list as "WASAPI: Speakers (Lochnagar USB Audio 2.0)". Lochnagar 2.0 supports both Event and Push modes; Microsoft recommends using Event mode where possible.

It is recommended to use ASIO over WASAPI if multichannel or bit-exact audio is required.

7.4 Using Lochnagar 2 with ASIO

ASIO drivers for Windows are installed as part of the Lochnagar 2 Device Pack.

Using ASIO will allow up to 16 channels (full duplex) to be transferred to and from the Lochnagar 2 board and provides higher bandwidth, lower latency, less jitter and un-mixed/un-distorted audio that bypasses the Windows Kernel Mixer. However, this requires specialist audio software such as Adobe Audition to interface with the ASIO drivers. This section will detail how to set up Lochnagar 2 on both Adobe Audition and Foobar.

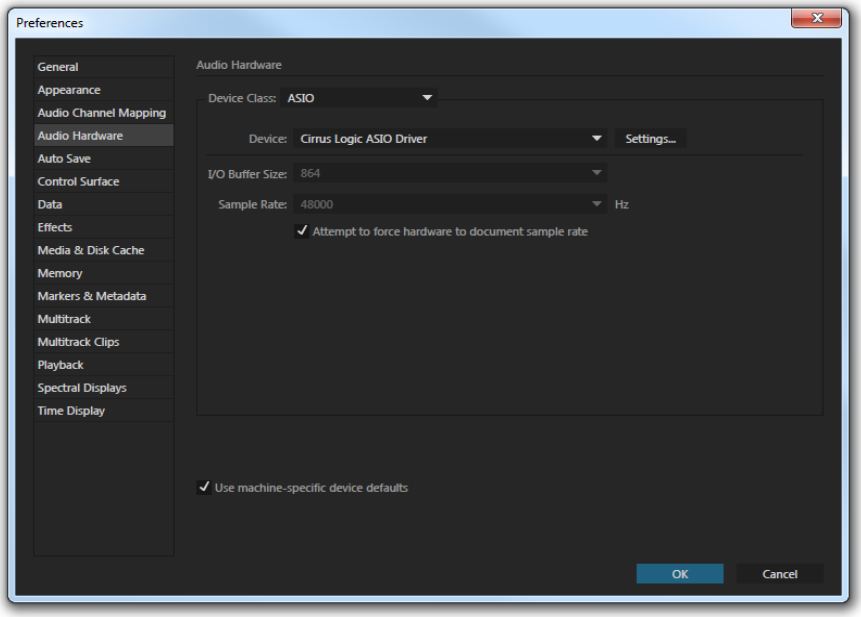
8 kHz Sampling Rate

Full bit accuracy cannot be guaranteed when using a sampling rate of 8 kHz, as there is a risk of losing some samples in the USB transfer.

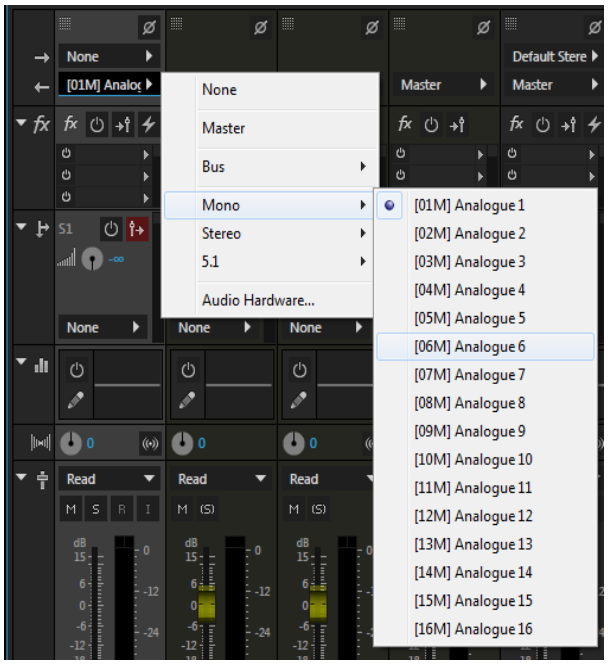
7.4.1 Adobe Audition Setup

In order to use Lochnagar 2 with ASIO on Windows, an ASIO-compatible sound editor is required. For this example, Adobe Audition is used, but setup on other editors should be very similar.

1. Enter the Audio Hardware panel in the Preferences box.
2. Select "ASIO" as the Device Class
3. Select "Cirrus Logic ASIO Driver" as the Device
4. Tick the "Attempt to force hardware to document sample rate" box, if it is present in your version of Audition
   a. If this option is not available, you will need to use the Windows Control Panel to set hardware sample rate.
5. Click "OK" to save changes



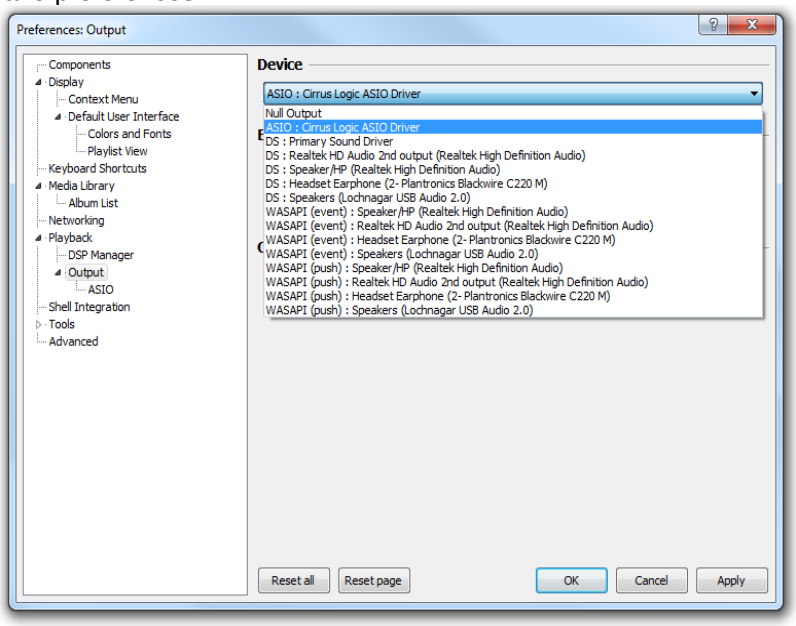
When selecting an output channel for each track in the project, there will now be 16 available input and output channels to select.



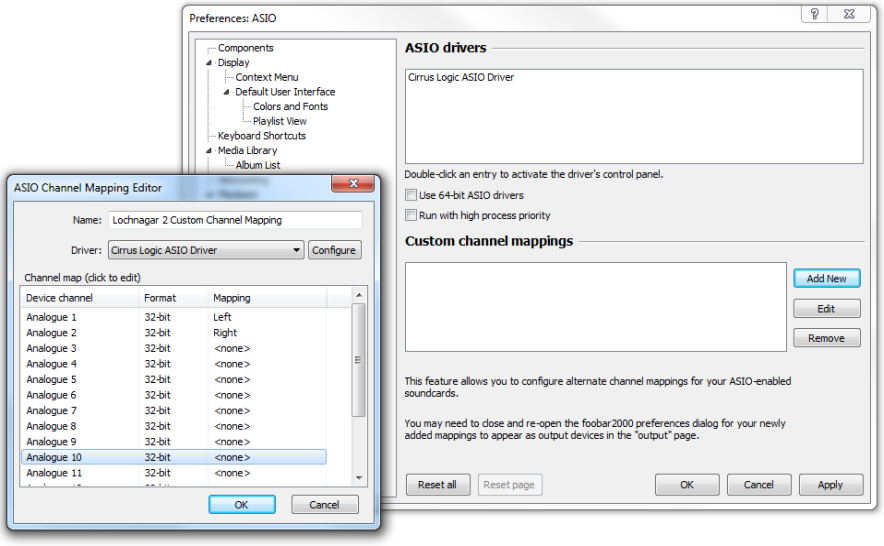
7.4.2 Foobar Setup

Foobar is a free media player which also offers ASIO support, although its multi-channel support is limited. However, it may be preferable in many instances since it is free to download and does not require a license or subscription.

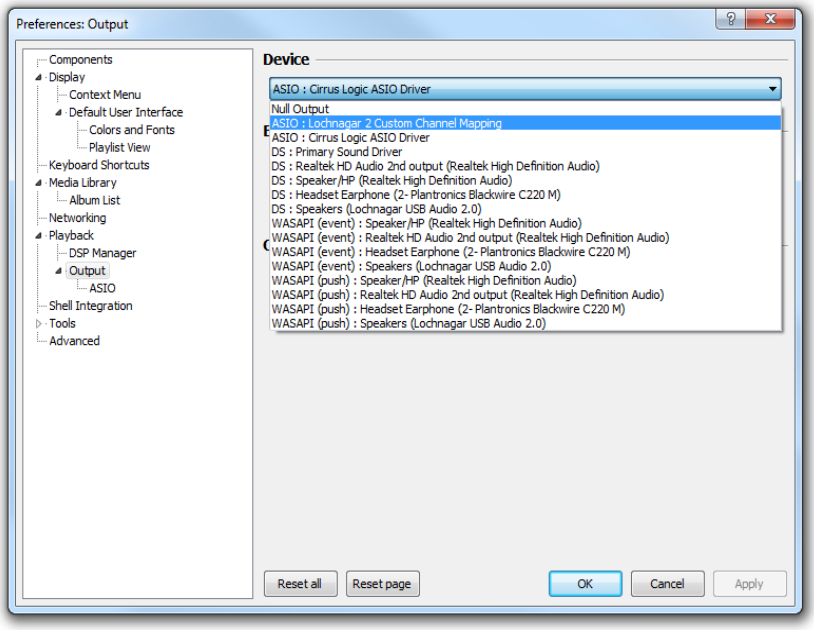
1. Download and install Foobar if required: http://www.foobar2000.org/download
2. Download the and install the ASIO plugin for Foobar: http://www.foobar2000.org/components/view/foo_out_asio
3. Go to File->Preferences->Playback->Output. Select "ASIO: Cirrus Logic ASIO Driver" from the drop-down list of devices. Click "OK" to save preferences.



4. The default channel mapping maps the audio's Left channel to ASIO output channel 1, and Right channel to ASIO output channel 2. These mappings can be re-mapped by entering the 'ASIO' sub-panel of the Output preferences and creating a custom channel mapping.



5. Once a custom channel mapping has been created, it can be selected from the drop-down Device select list on the main Output preferences panel.



> *Note that Foobar allows for multichannel ASIO output, but the source file must be encoded as a multi-channel (eg. 5.1) file - it cannot play two stereo files simultaneously to four different ASIO output channels like Adobe Audition can.*

7.5 I2S Format on Lochnagar 2

Regardless of which audio driver type is used, the onboard USB audio streamer device will convert the 16 channels of audio data from the PC into two data streams, each in 8-channel I2S format. Each set of 8 channels can be routed separately to any AIF interface on the board.

- **USB AIF Channels[1-8]** maps to ASIO channels 1-8
- **USB AIF Channels[9-16]** maps to ASIO channels 9-16

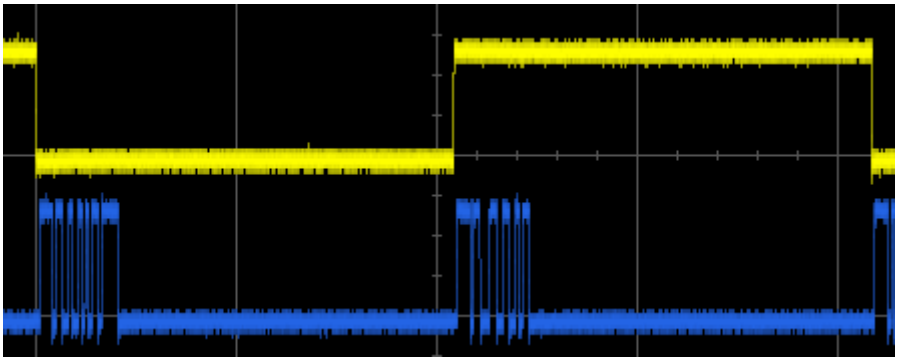
The output format from the USB streaming peripheral will use an 8-channel I2S format, even if only 2/4/6 channels are actively transmitted or received from the PC. The USB streamer will always be the master of the BCLK and LRCLK signals, as the sampling rate will be dictated by the CLUSBAudio driver. When the USB streaming audio is routed to a Cirrus Logic Smart Codec AIF peripheral, the AIF port of the Cirrus Logic device should be configured as a slave and should expect data in this format.

When using 176.4 kHz or 192 kHz sampling rate, the number of channels drops to a supported maximum of 8 channels in each direction, which is presented to the minicards as two separate 4-channel I2S streams. The CLUSBAudio Driver format selection must be reconfigured to "8 channels, 24 bits" for both input and output when using 176.4 kHz or 192 kHz sampling rates or it will not function correctly. When using these rates with the "8 channels, 24 bits" selection in the driver, the I2S channel routings are mapped as:

- **USB AIF Channels[1-8]** maps to ASIO channels 1-4
- **USB AIF Channels[9-16]** maps to ASIO channels 5-8

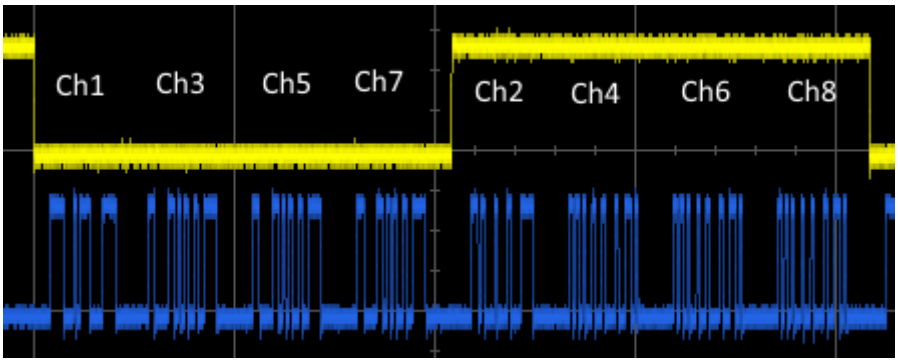
Note that this channel mapping is dependent on the sampling rate only, not on the format selection in the CLUSBAudio Driver. If the "8 channels, 24 bit format" is selected in CLUSBAudio when operating with sampling rates lower than 176.4 kHz, all eight channels will be mapped to the same 8-channel I2S channel on USB AIF Channels[1-8] and channels 9-16 will be unusable.

Stereo data transferred to Lochnagar 2



The USB audio output will always be in 8 channel I2S format, even when using stereo data audio in DirectSound mode.

8 channel data transferred to Lochnagar 2 via ASIO



When using the AIF routing option USB AIF Channels[1-8], the channel number shown in the image map directly to the ASIO channel numbers (eg "Analogue 1") as seen in Adobe Audition screenshots above. When using AIF routing option USB AIF Channels[9-16], the 8 channels of I2S map to ASIO channels 9-16 rather than 1-8.

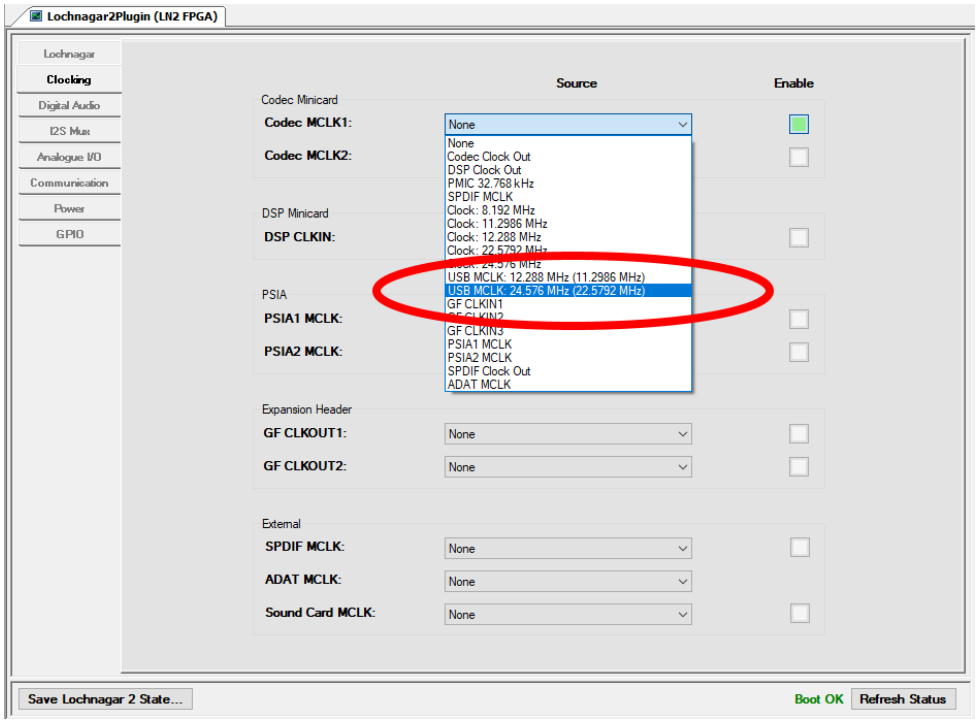
7.6 Lochnagar 2 USB Audio BCLK Rates

The USB audio streaming peripheral will always master the BCLK and LRCLK signals on the I2S bus, and the sampling rate will be dictated by the PC side through the audio drivers. This means that the BCLK generated by the USB audio streamer will be determined by the sampling rate settings on the PC.

Sample rate (Hz)	I2S Channel Count per AIF	BCLK Frequency (Hz)
8000	8	2048000
16000	8	4096000
22050	8	5644800
24000	8	6144000
32000	8	8192000
44100	8	11289600
48000	8	12288000
88200	8	22579200
96000	8	24576000
176400	4	22579200
192000	4	24576000

7.7 USB MCLK

USB MCLK is available as either 24.576 MHz (22.5792 MHz) or 12.228 MHz (11.2986 MHz). Both options are synchronous with the I2S digital audio generated by the USB Audio Subsystem. The USB MCLK will change between the 48 kHz and 44.1 kHz sample rate families automatically when the sample rate on the USB host machine changes.

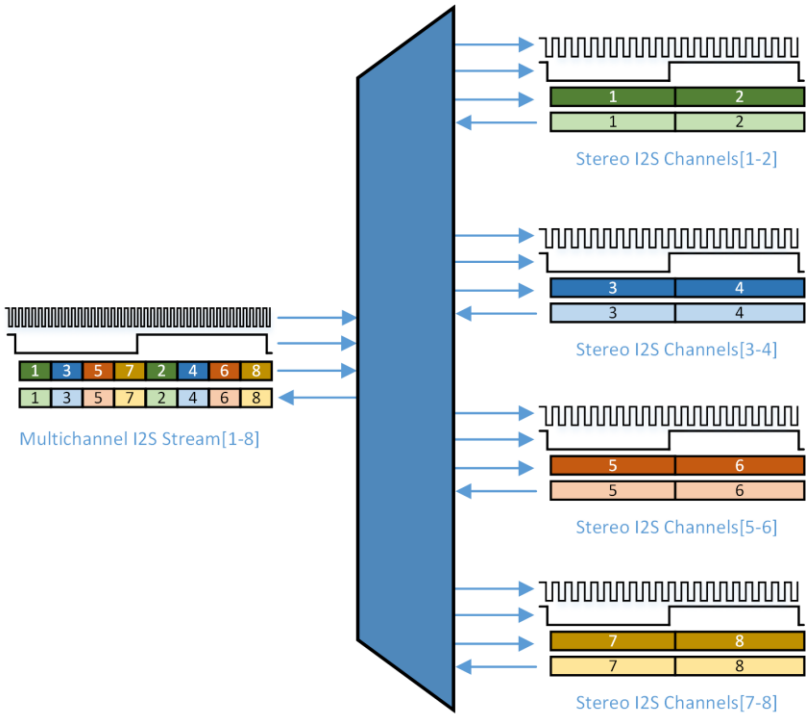


8 I2S Mux

The Lochnagar 2 FPGA provides a peripheral block that will convert time domain multiplexed 8-channel I2S data into stereo I2S streams and vice versa.

The Lochnagar 2 USB Audio Streaming peripheral always operates using 8-channel I2S audio data with 32-bit audio slots (or 4-channel at 192 kHz) and in some cases this may be undesirable. For example, running with a faster BCLK than is required will slightly increase the power consumption on the digital buffer voltage supply rail, and for power sensitive applications this may be undesirable. For this purpose, the Lochnagar 2 board can convert 8-channel 256Fs I2S data into four separate streams of stereo 64Fs I2S data that can be routed to four separate destinations on the Lochnagar 2 board. Similarly, the return data from the four separate I2S streams can be combined into a single 8-channel I2S return channel. If 4-channel 128Fs I2S data is provided on the multichannel side, the block will function in the same way but the stereo I2S inputs and outputs for channels 5-8 will not be used.

8.1 I2S Mux/Demux Operation

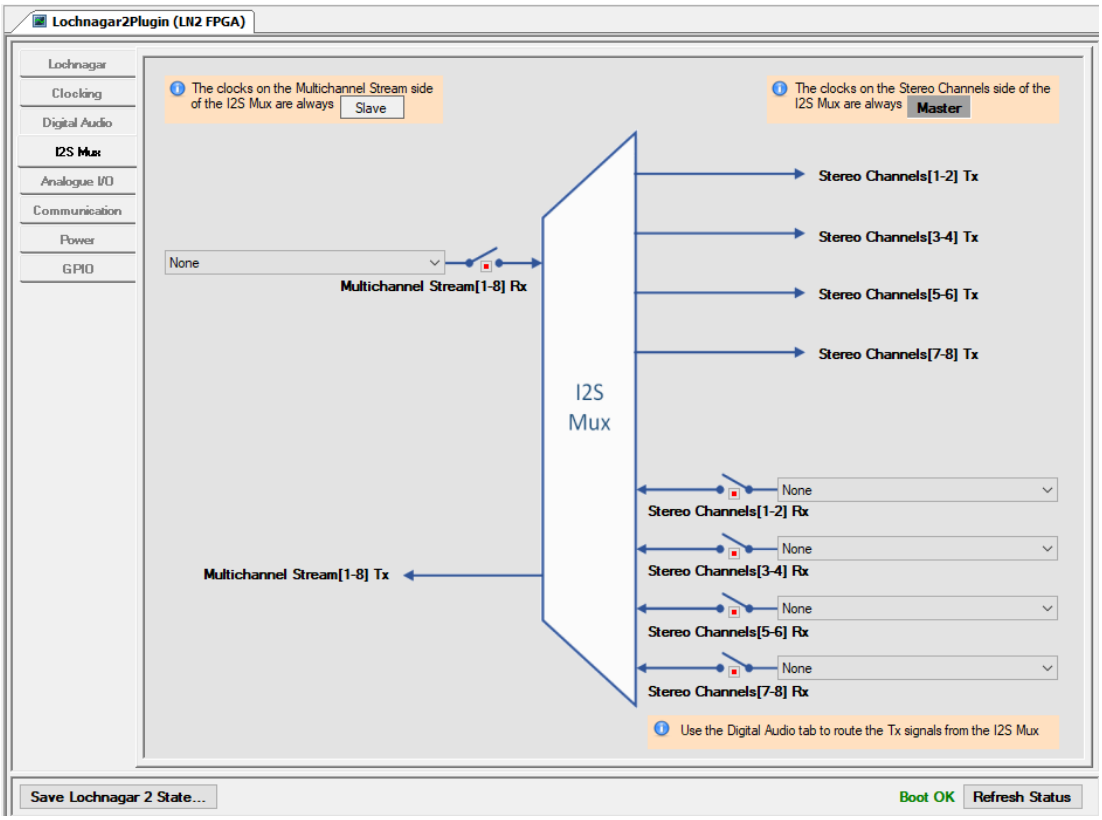


The I2S Mux peripheral splits an 8-channel I2S stream into four separate stereo I2S buses. The peripheral assumes an audio channel size of 32-bits and will extract the data using that assumption. The clocks on the demuxed stereo streams are derived from the clocks on the multichannel side, so they will always function as I2S masters with respect to their destinations. The derived BCLK signals on the stereo side will be four times slower than the BCLK on the multichannel side.

It is possible to use as many or as few of the stereo I2S streams as is required by the end use case.

8.2 Configuring the I2S Mux Peripheral

The I2S Mux/Demux is configured through the **I2S Mux** and **Digital Audio** tabs of the Lochnagar 2 Plugin. These two tabs must be used in combination to configure the I2S Mux peripheral.



8.2.1 Example Configuration

This section will describe the steps required to connect the Lochnagar 2 USB audio streaming to the Codec AIF1 port through the I2S Mux peripheral. This will extract channels 1 and 2 of the 8-channel USB audio data and present it to Codec AIF1 as a stereo 64Fs I2S data stream. The stereo return data from the Codec AIF1 will be returned back to the USB streaming peripheral as an 8-channel I2S signal from the I2S Mux/Demux peripheral.

1. Set up the Codec MCLK using the **Clocking** panel of the Lochnagar 2 Plugin. As the data is coming from the USB audio streaming peripheral, one of the USB MCLK signals should be routed to Codec MCLK1. This could be either the 24.576 MHz or 12.288 MHz variant, as both are synchronous with the USB audio data.
2. On the **I2S Mux** panel, select the Multichannel Stream[1-8] Rx source as USB AIF Channels[1-8] Tx.
3. Click the Enable switch button next to the Multichannel Stream[1-8] Rx source selector box. This changes color from red to green.
4. Select the Stereo Channels[1-2] Rx source as Codec AIF1 Tx. This routes the return data from the codec back through the I2S Mux peripheral.
5. On the **Digital Audio** panel, Select the Codec AIF1 Rx Source as I2S Mux Stereo Channels[1-2] Tx. This routes the stereo data from the I2S Mux peripheral to the Codec AIF1.
6. Set the Codec AIF1 LRCLK and BCLK signals to Slave mode. This means that these clocks will be supplied by the I2S Mux peripheral.
7. Click the Enable button on the Codec AIF1 row.
8. Select the USB AIF Channels[1-8] Rx Source as I2S Mux Multichannel Stream[1-8] Tx. This connects the 8-channel return path from the I2S Mux to the USB audio streaming peripheral.
9. Make sure the BCLK and LRCLK are set to Master mode in order to provide these clocks to the I2S Mux peripheral. USB Audio Streaming always operates in this mode, so no action is required in this example.

10. Set the High Frequency Mode setting for the USB AIF Channels[1-8] to Buffered mode to compensate for increased path delay in the I2S Mux peripheral.
11. Click the Enable button on the USB AIF Channels[1-8] row.

This setup is provided as one of the example scripts in the Lochnagar 2 Device Pack profile scripts directory.

8.2.2 Description of I2S Sinks and Sources

The I2S Mux/Demux is integrated with the Digital Audio routing functionality and has access to the full range of audio sources as any of the other AIF digital audio.

All I2S Mux use cases will require both **Digital Audio** and **I2S Mux** panels of the Lochnagar 2 Plugin, as the functionality is heavily interlinked.

8.3 Clocking Restrictions

LRCLK and BCLK for the I2S Mux/Demux peripheral are provided by the AIF source that is selected as the Multichannel Stream[1-8] Rx source. This source is selected on the left side of the **I2S Mux** plugin tab. The corresponding AIF port must be set as BCLK and LRCLK Master on the **Digital Audio** tab of the plugin, otherwise no clocks will be provided to the I2S Mux block.

Any AIF ports connected to the stereo inputs/outputs of the I2S Mux block must be set as BCLK and LRCLK Slave ports on the **Digital Audio** page of the plugin, otherwise there will be a conflict as two clocks drive against each other.

Note that since the I2S Mux block is bidirectional, it is possible to connect different AIF ports to the upstream and downstream audio on each of the stereo and multichannel sides. That is, the AIF port selected as the Multichannel Stream[1-8] Rx Source must be set up as a clock Master, but this does not necessarily have to be the AIF port that receives the Multichannel Stream[1-8] Tx data. Due to the clocking restrictions about which ports can be masters/slaves, this can get confusing and such use cases must be treated with care.

High Frequency Mode

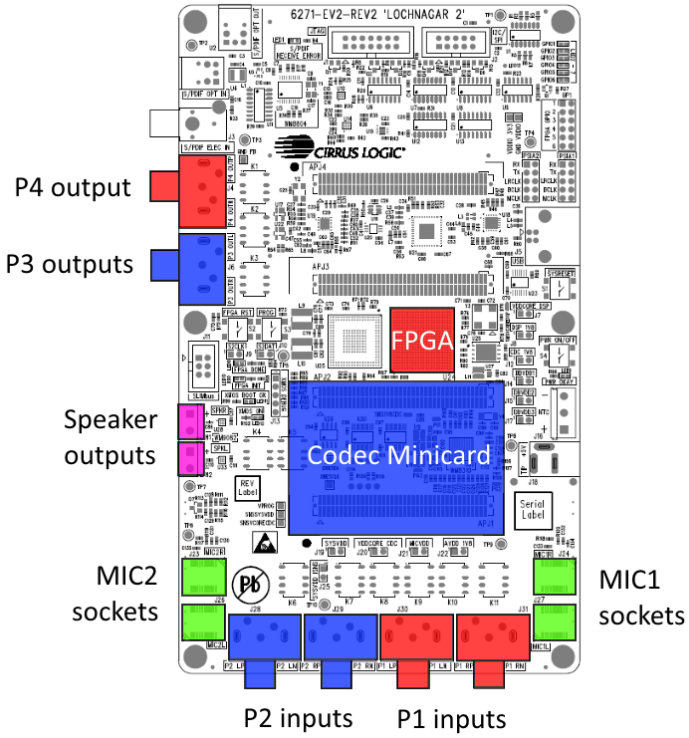
When using the I2S Mux block functionality, it is highly recommended to enable Buffered mode on the AIF Master that provides the I2S Mux peripheral with its BCLK and LRCLK.

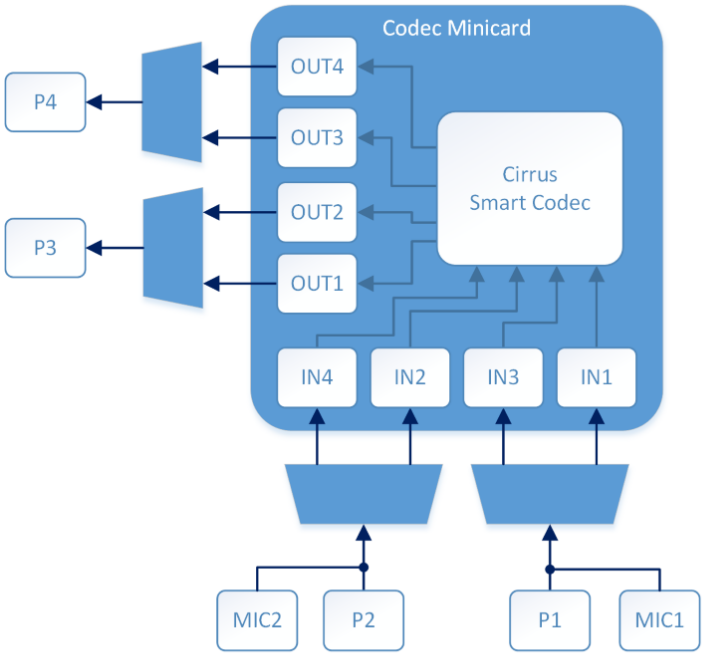
The I2S Mux block will add extra latency into the audio path, and this may be enough to corrupt the return data for audio streams with high BCLK rates or long PCB traces. Enabling buffered mode will compensate for some of this extra round trip delay.

9 Analog Audio

This section details the analog audio inputs and outputs on the Lochnagar 2 board, and how to configure the routing. Analog inputs and outputs are routed directly to the audio codec minicard through relays and switches. The FPGA registers control the positions of the relays, thus determining how the analog I/O is connected to the Cirrus Logic Smart Codec device.

9.1 Analog Port Connection Diagrams

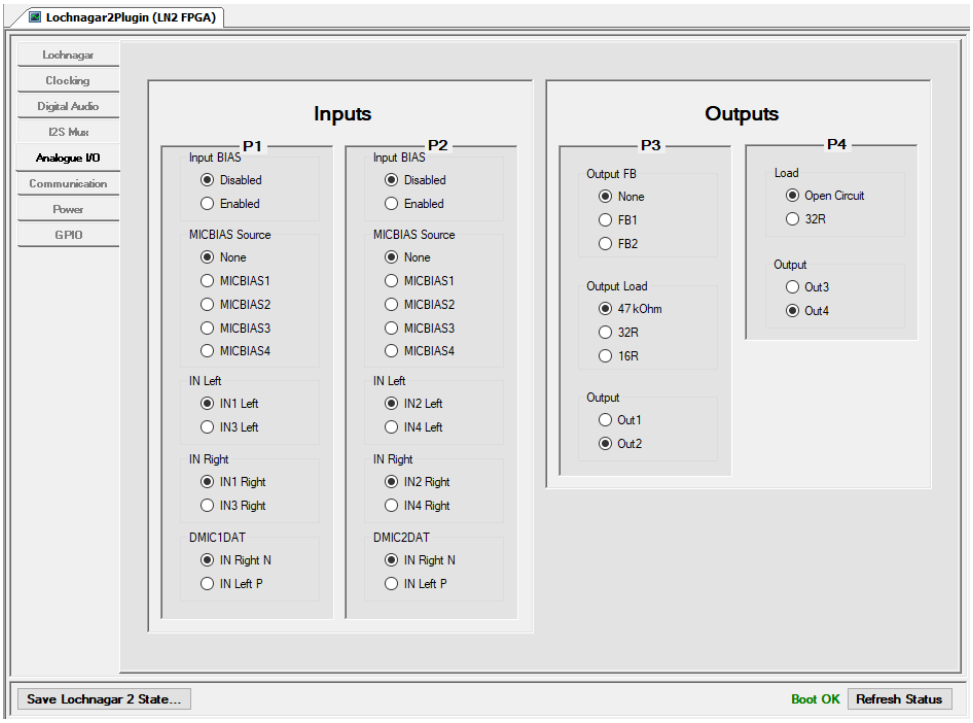




> *Note that for some codec minicards, certain inputs and outputs may be unavailable, or may be used to support other features on the minicard itself. It is therefore important to check the minicard schematic to see exactly how the input and output signals are connected to the device on the minicard PCB. Newer codec WISCE™ Device Pack installers may provide meta-data to the Lochnagar 2 Plugin, allowing it to display some of this context-dependent routing information.*

9.2 Configuring Analog Audio Routing

Routing the various analog audio options can be done through the **Analogue I/O** page of the Lochnagar 2 Plugin.



9.2.1 Saving Analog Routing State

The analog I/O registers must be written to in a certain sequence for the changes to be effective. This will involve a small time delay for the relay switches on the board to change state.

To replicate the current state of the Lochnagar 2 board, it is recommended to use the "**Save Lochnagar 2 State...**" button at the bottom of the Plugin window to generate a WISCE™ profile script that includes this sequencing.

9.3 RCA Phono Input Ports

There are two sets of phono input ports, P1 and P2, each consisting of stereo differential pair signals (Positive and Negative signals for each of Left and Right channels). These phono connectors are directly tied to the microphone input sockets, so P1 cannot be used if there are microphones plugged into either or both of the MIC1 sockets and P2 cannot be used if there is a microphone plugged into either or both of the MIC2 sockets.

9.3.1 P1 phono inputs

P1 consists of four RCA phono inputs:

- P1 LP (red)
- P1 LN (white)
- P1 RP (red)
- P1 RN (white)

P1 can be used as either two single-ended inputs (usually using P1 LN and P1 RN, the white connectors on the upper side) or as two full differential inputs (using P1 LP and LN for the left channel input, and P1 RP and RN for the right channel input).

P1 will connect to either of the following input channels on the codec minicard:

- IN1
- IN3

Each of the left and right channels can be routed separately (for example P1 left channel can go to IN1 while P1 right channel goes to IN3). This selection is made in the plugin.

Note that for some codec minicards, certain inputs may be unavailable, or may be used for other features (eg. headset feedback signals). It is therefore important to check the minicard schematic to see exactly how the input signals are connected on the minicard PCB. Newer codec WISCE™ Device Pack installers may provide meta-data to the Lochnagar 2 Plugin, allowing it to display some of this context-dependent routing information.

9.3.2 P2 phono inputs

P2 consists of four RCA phono inputs:

- P2 LP (red)
- P2 LN (white)
- P2 RP (red)
- P2 RN (white)

P2 can be used as either two single-ended inputs (usually using P2 LN and P2 RN, the white connectors on the upper side) or as two full differential inputs (using P2 LP and LN for the left channel input, and P2 RP and RN for the right channel input).

P2 will connect to either of the following input channels on the codec minicard:

- IN2
- IN4

Each of the left and right channels can be routed separately (for example P2 left channel can go to IN2 while P2 right channel goes to IN4).
This selection is made in the plugin.

Note that for some codec minicards, certain inputs may be unavailable, or may be used for other features (eg. headset feedback signals). It is therefore important to check the minicard schematic to see exactly how the input signals are connected on the minicard PCB. Newer codec WISCE™ Device Pack installers may provide meta-data to the Lochnagar 2 Plugin, allowing it to display some of this context-dependent routing information.

9.3.3 Input BIAS

It is possible to connect a MICBIAS voltage directly to the P channels of the RCA phono inputs by enabling the "Input BIAS" feature in the Lochnagar 2 Plugin. This connects the RCA inputs to the MICBIAS voltage selected in the "MICBIAS Source" selection and allows external ECM microphones to be connected to the RCA connectors. See section 0 for more details.

9.4 Analog/Digital Microphones

The microphone sockets MIC1 and MIC2 allow up to four digital or analog microphone mincards (also referred to as 'MIC coupons'). The full range of Cirrus Logic analog and digital microphones can be connected to the Lochnagar 2 system.

- The MIC1 sockets are directly tied to the P1 analog RCA inputs - if the MIC1 sockets are in use, then the P1 RCA connectors cannot be used.
- The MIC2 sockets are directly tied to the P2 analog RCA inputs - if the MIC2 sockets are in use, then the P2 RCA connectors cannot be used.

The routing options selected for P1 and P2 within the plugin will apply to the microphone inputs as they would to the RCA analog inputs.

9.4.1 MICBIAS

The microphone sockets can be powered from one of up to four MICBIAS outputs on the Codec Minicard. This selection is made within the plugin.

Mic socket	MICBIAS Source options
MIC1 (P1)	• None • MICBIAS1 • MICBIAS2 • MICBIAS3 • MICBIAS4
MIC2 (P2)	• None • MICBIAS1 • MICBIAS2 • MICBIAS3 • MICBIAS4

> *Note that some codec minicards may not have four MICBIAS outputs due to limitations of certain Cirrus Logic Smart Codec devices. It is therefore important to always check the minicard schematic to see exactly how the output signals are connected on the minicard PCB. Newer codec WISCE™ Device Pack installers may provide meta-data to the Lochnagar 2 Plugin, allowing it to display some of this context-dependent routing information.*

9.4.2 Analog Microphones

When used with an analog microphone coupon, the inputs will be connected as follows:

Mic socket	Minicard connector
MIC1L	Differential P1 INLP and P1 INLN
MIC1R	Differential P1 INRP and P1 INRN
MIC2L	Differential P2 INLP and P2 INLN
MIC2R	Differential P2 INRP and P2 INRN

> *Note that for some codec minicards, the connections from P1 and P2 may be routed to differently numbered input pins on the Cirrus Logic Smart Codec itself. It is therefore important to always check the minicard schematic to see exactly how the output signals are connected on the minicard PCB. Newer codec WISCE™ Device Pack installers may provide meta-data to the Lochnagar 2 Plugin, allowing it to display some of this context-dependent routing information.*

9.4.3 Digital Microphones

When used with a digital microphone coupon, the inputs will be connected as follows, depending on the DMICnDAT_SEL setting:

Mic socket	DMICDAT_SEL = 0	DMICDAT_SEL = 1
MIC1L and MIC1R	Clock: P1 INLN, Data: P1 INRN	Clock: P1 INLN, Data: P1 INLP
MIC2L and MIC2R	Clock: P2 INLN, Data: P2 INRN	Clock: P2 INLN, Data: P2 INLP

Both left and right channel microphones use the INLN and INRN connectors. The stereo data signals are transmitted on either positive or negative clock edges depending on which of the MICnL/MICnR sockets the coupon is plugged into.

Some Smart Codec devices require the DMIC data signal to be connected to the the INRN analog input on the Smart Codec, and some require that it connects to the INLP pin. Lochnagar 2 provides a relay switch that allows it to be connected to either of these input pins on the Smart Codec minicard. There will therefore be a required DMICDAT_SEL setting for each minicard that routes the DMICDAT signals to the appropriate pins.

> *Note that for some codec Minicards, the connections from P1 and P2 may be routed to differently numbered input pins on the Cirrus Logic Smart Codec itself. It is therefore important to always check the minicard schematic to see exactly how the output signals are connected on the minicard PCB. Newer codec WISCE™ Device Pack installers may provide meta-data to the Lochnagar 2 Plugin, allowing it to display some of this context-dependent routing information.*

9.5 RCA Phono Output Ports

There are two sets of phono output ports, P3 and P4. P3 is a stereo single-ended output pair, P4 is a mono differential output.

9.5.1 P3 phono outputs

P3 is a pair of single-ended RCA phono outputs:

- P3 OUTR (red)
- P3 OUTL (white)

P3 can be connected to either of the following output channels on the codec minicard:

- OUT1
- OUT2

> *Note that for some codec minicards, certain outputs may be unavailable, or may not be routed down to the Lochnagar 2 board. It is therefore important to check the minicard schematic to see exactly how the output signals are connected on the minicard PCB. Newer codec WISCE™ Device Pack installers may provide meta-data to the Lochnagar 2 Plugin, allowing it to display some of this context-dependent routing information.*

9.5.1.1 Output FB

The feedback signal from P3 can be routed back to one of the following minicard feedback pins:

- FB1
- FB2
- None

9.5.1.2 Output Load

The P3 output signals can have one of the following loads applied:

- 47 kOhm
- 32 Ohm
- 16 Ohm

9.5.2 P4 phono output

P4 is a single channel differential RC phono output:

- P4 OUTN
- P4 OUTP

P4 can be connected to either of the following output channels on the codec minicard:

- OUT3
- OUT4

> *Note that for some codec minicards, certain outputs may be unavailable, or may not be routed down to the Lochnagar 2 board. It is therefore important to check the minicard schematic to see exactly how the output signals are connected on the minicard PCB. Newer codec WISCE™ Device Pack installers may provide meta-data to the Lochnagar 2 Plugin, allowing it to display some of this context-dependent routing information.*

9.5.2.1 Output Load

The P4 output signals can have one of the following loads applied:

- None (Open-circuit/CCT)
- 32 Ohm

9.6 Speaker Outputs

Lochnagar 2 is equipped with two screw-terminal speaker outputs, SPKL and SPKR which are powered by discrete Cirrus Logic WM9082 speaker amplifiers. The central Lochnagar 2 FPGA can route PDM output signals from the codec minicard to these terminals. The speaker outputs are connected to the PDM output 1 pins from the codec minicard.

9.7 Analog I/O on the minicard

Most Smart Codec audio minicards provide several analog output ports. These usually consist of:

- 4-pole 3.5 mm Headset connector
- Earpiece output (screw terminals)
- Speaker outputs (screw terminals)

This will vary from minicard to minicard, so it is important to check the minicard schematics.

> *Minicards with a headset connector will often use one of the Cirrus Logic device's analog inputs to provide a feedback signal for the headphone connector. This means that it may not be possible to use that particular analog input at the same time as using the headset output on the minicard. Check the minicard schematics to see which analog input ports are affected by minicard board routing. Newer codec WISCE™ Device Pack installers may provide meta-data to the Lochnagar 2 Plugin, allowing it to display some of this context-dependent routing information.*

10 GPIOs

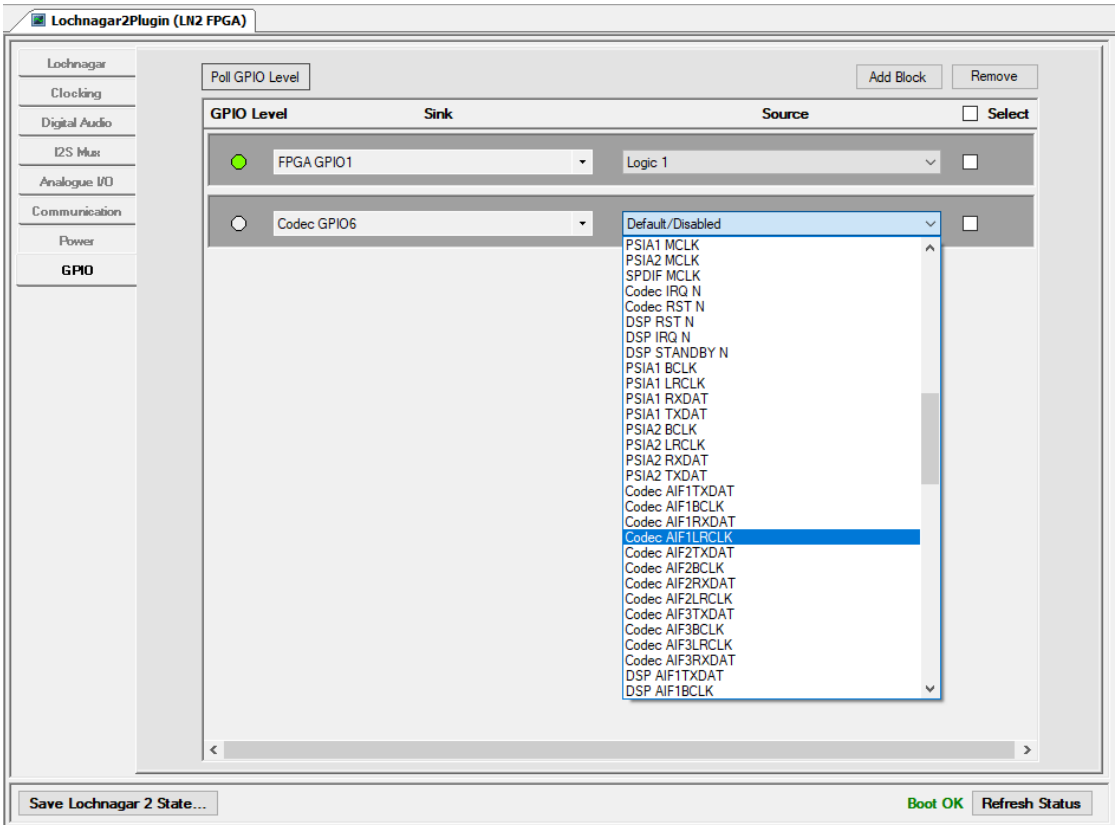
Lochnagar 2 provides advanced GPIO routing support that allows the full flexibility of any-to-any pin mapping.

With the increases in flexibility in GPIO usage that chips such as the CS47L85 and CS47L90 bring over previous generations, Lochnagar 2 now also provides a similar level of control at the board level. On the CS47L85 onwards, there are several dedicated GPIO pins per chip, and in addition most digital I/O can also be used in GPIO mode, giving up to 40 potential GPIO signals per chip. Lochnagar 2 allows any of these pins to be used in GPIO mode and allows them to be routed to any other digital I/O, regardless of the pin's default function.

Lochangar 2 allows for up to 16 pairs of pins to be mapped as GPIOs at any one time.

10.1 Setting up GPIO Routing

GPIO routing setup is controlled through the **GPIO** panel of the Lochnagar 2 Plugin.



1. Select the GPIO panel to begin setting up any-to-any pin GPIO connections.
2. Select "Add Block" to create a connection between two GPIO pins
3. Select the "Sink" from the left-hand drop-down list. The FPGA will actively drive onto this pin as an output
4. Select the "Source" from the right-hand drop-down list. The FPGA will use this pin as an input, and map the values onto the Sink pin.
5. If a GPIO connection is no longer required, mark the checkbox next to the connection and click the "Remove" button.

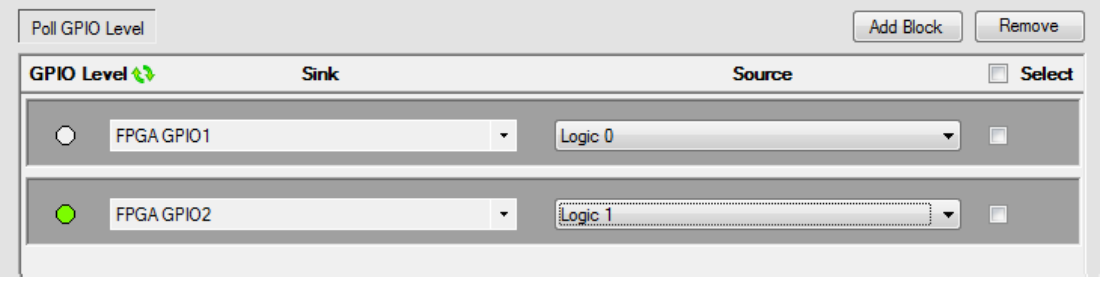
> *Note that if a GPIO pin on the system is used by another function, such as a digital audio interface, the plugin will highlight the Digital Audio panel and display warnings to indicate that one of the digital audio pins is being used as a GPIO and may not function correctly.*

10.2 GPIO Level

The Lochnagar 2 can display the current logic level for all signals that are routed through the GPIO system.

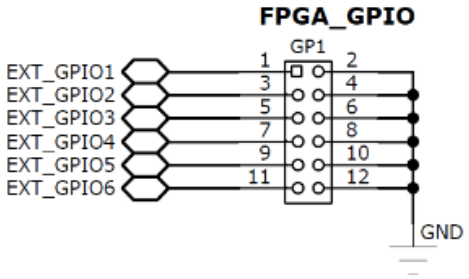
To enable this feature, click the "Poll GPIO Level" button in the top-left corner of the plugin's GPIO panel. The logic high/low level for each GPIO will be displayed in the green circle to the left of the GPIO sink. The green arrows next to "GPIO Level" indicate that the plugin is currently polling, and the logic states shown in the plugin are up-to-date.

Note that enabling this feature will generate a lot I2C traffic in the WISCE™ history window as the plugin polls the Lochnagar 2 board to read the current logic levels. The refresh rate will depend on many elements including PC speed and amount of other USB traffic on the bus.

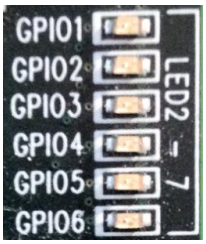


10.3 Lochnagar 2 On-Board GPIOs/LEDs

Lochnagar 2 has six dedicated GPIO pins for debug purposes, which are accessible through the GP1 header on the top-Lochangar 2 has six dedicated GPIO pins for debug purposes, which are accessible through the GP1 header on the top-right corner of the board. These are listed in the plugin and register map as **FPGA GPIO1** to **FPGA GPIO6**.



The six dedicated GPIOs are tied directly to the bank of six LEDs in the same corner of the Lochnagar 2 board, such that the logic values on the GPIOs can be observed visually without the need for an oscilloscope. The value on the pins can also be read back by software. This is done by setting up "FPGA GPIOn" as a GPIO sink and enabling the polling feature from the Lochnagar 2 Plugin.



The Lochnagar 2 GPIO pins operate on the 3.3V voltage domain.

10.4 GPIOs on Codec Minicards

Codec minicards have reserved pins for up to eight dedicated GPIO signals from the Cirrus Logic Smart Codec. The positions of the shared-function GPIO pins will change from chip to chip, so GPIO16 may be an AIF pin on some devices or a PDM pin on others. For this, it is vital to check the device datasheet to correlate GPIO numbers & pin functions.

It is also worth noting that some devices have less than eight dedicated GPIO pins and therefore these signals will be left floating on the minicard.

Depending on the minicard design, it is probable that the schematic will be using at least one of the eight available GPIO pins on the Cirrus Logic Smart Codec for a fixed function such as clock output or headset polarity switching. As such, even if the device has eight dedicated GPIO pins, it is likely that only a subset of these GPIO pins will be routed down to the Lochnagar 2 board & FPGA. For this reason, it is vital to consult the schematics for the minicard to ensure that the GPIO in question is actually connected.

10.5 Descriptions of GPIO Sinks and Sources

This section lists and describes the pins that can be used as GPIO sinks and GPIO sources using the Lochnagar 2.

10.5.1 GPIO Sink List

The sink list chooses which pin to use as a GPIO. This may be a dedicated GPIO pin, or a digital I/O pin that has an alternate function (eg. digital audio BCLK pin). This pin will be driven as an output from the FPGA with the value of the source signal selected in the GPIO source list. The register map addresses associated with these GPIO sinks is provided for advanced users.

Name	Related Registers	Description
None		No GPIO sink has been selected
FPGA GPIOn	R31h - R36h	Drives out onto one of the 6 pins on the GPIO Header / LED Bank
Codec GPIOn	R37h - R3Eh	Drives out onto one of the 8 dedicated GPIO pins on the Codec Minicard
DSP GPIOn	R3Fh - R44h, R9Ah	Drives out onto one for the dedicated GPIO pins on the DSP Minicard
GF GPIOn	R45h - R47h, R98h - R99h	Drives out onto one of the dedicated GPIOs on the underside Expansion Headers
Codec AIFnBCLK/RXDAT/LRCLK/TXDAT	R48h - R53h	Drives out onto the AIF pins on the Codec Minicard
DSP AIFnBCLK/RXDAT/LRCLK/TXDAT	R54h - R5Bh	Drives out onto the AIF pins on the DSP Minicard
PSIAn BCLK/RXDAT/LRCLK/TXDAT	R5Ch - R63h	Drives out onto the pins on the PSIA headers
GF AIFnBCLK/RXDAT/LRCLK/TXDAT	R64h - R73h	Drives out onto the AIF pins on the underside Expansion Header
DSP UARTn RX/TX	R74h - R77h	Drives out onto the UART pins on the DSP Minicard
GF UART2 RX/TX	R78h - R79h	Drives out onto the UART pins on the underside Expansion Header
USB UART RX	R7Ah	Drives out onto the UART RX pin of the Generic USB UART device
Codec PDMCLK/DATn	R7Ch - R7Fh	Drives out on the PDM pins on the Codec Minicard
Codec DMICCLK/DATn	R80h - R87h	Drives out onto the DMIC pins on the Codec Minicard
DSP DMICCLK/DATn	R88h - R8Bh	Drives out onto the DMIC pins on the DSP Minicard
I2Cn SCL/SDA	R8Ch - R91h	Drives out onto the I2C pins of systemwide I2C buses 2, 3 or 4
DSP STANDBY N	R92h	Drives out onto the 'standby' pin on the DSP Minicard
Codec MCLKn	R93h - R94h	Drives out onto the MCLK pins on the Codec Minicard
DSP CLKIN	R95h	Drives out onto the CLKIN pin on the DSP Minicard
PSIAn MCLK	R96h - R97h	Drives out onto the MCLK pins on the PSIA headers
External JTAG TDO	R9Bh	Drives out onto the JTAG TDO pin on the External JTAG Header
USB JTAG TDO	R9Ch	Drives out onto the JTAG TDO pin on the USB JTAG device

10.5.2 GPIO Source List

The logic value on the selected source will be will be applied to the GPIO sink pin selected in the GPIO sink list. The binary values are provided for advanced users.

Name	Binary Value	Description
Default/Disabled	0x00	Not used as a GPIO
FPGA GPIOn	0x00 - 0x06	Connects to one of the 6 pins on the Lochnagar 2 GPIO Header / LED Bank
Codec GPIOn	0x07 - 0x0E	Connects to one of the 8 dedicated GPIO pins on the Codec Minicard
DSP GPIOn	0x0F - 0x14, 0x1A	Connects to one of the dedicated GPIO pins on the DSP Minicard
GF GPIOn	0x15 - 0x19	Connects to one of the dedicated GPIOs on the underside Expansion Headers
Codec Clock Out	0x20	Connects to the clock output pin of the Codec Minicard
DSP Clock Out	0x21	Connects to the clock output pin of the DSP Minicard
PMIC 32.768 kHz	0x22	Connects to the 32.768 kHz output clock from the PMIC chip
SPDIF Clock Out	0x23	Connects to the 12 MHz output clock from the S/PDIF Transceiver chip
Clock: 8.192 MHz	0x28	Connects to the 8.192 MHz clock from the onboard clock generator chip
Clock: 12.288MHz	0x24	Connects to the 12.288 MHz clock from the onboard clock generator chip
Clock: 11.2986MHz	0x25	Connects to the 11.2986 MHz clock from the onboard clock generator chip
Clock: 24.576MHz	0x26	Connects to the 24.576 MHz clock from the onboard clock generator chip
Clock: 22.5792MHz	0x27	Connects to the 22.5792 MHz clock from the onboard clock generator chip
USB MCLK: 24.576 MHz (22.5792 MHz)	0x29	Connects to the USB MCLK: 24.576 MHz (22.5792 MHz) signal. Frequency will depend upon sampling rate of audio being transferred over USB. Will be either 24.576 MHz or 22.5792 MHz.
GF CLKOUTn	0x2A, 0x2E	Connects to the one of the clockout signals going to the underside Expansion Headers
GF CLKINn	0x2B, 0x2D, 0x2C	Connects to the MCLK signals coming from the underside Expansion Headers
Codec MCLKn	0x2F - 0x30	Connects to one of the 2 MCLK signals going to the Codec Minicard
DSP CLKIN	0x31	Connects to the CLKIN signal going to the DSP Minicard
PSIAn MCLK	0x32 - 0x34	Connects to the MCLK signals coming from / going to the PSIA headers
SPDIF MCLK	0x34	Connects to the MCLK signal coming from the S/PDIF transceiver. Frequency will depend upon the sampling rate of the audio.
Codec IRQ N	0x42	Connects to IRQ signal coming from the Codec Minicard
Codec RST N	0x43	Connects to hard reset signal going to the Codec Minicard
DSP RST N	0x44	Connects to hard reset signal going to the DSP Minicard
DSP IRQ N	0x45	Connects to IRQ signal coming from the Codec Minicard
DSP STANDBY N	0x46	Connects to Standby signal going to the Codec Minicard
PSIAn BCLK/LRCLK/RXDAT/TXDAT	0x50 - 0x57	Connects to the PSIA header pins
Codec AIFnTXDAT/BCLK/RXDAT/LRCLK	0x58 - 0x63	Connects to the AIF pins on the Codec Minicard
DSP AIFnTXDAT/BCLK/RXDAT/LRCLK	0x64 - 0x6B	Connects to the AIF pins on the DSP Minicard
GF AIF3RXDAT/BCLK/TXDAT/LRCLK	0x6C - 0x6F	Connects to the GF AIF3 pins on the underside Expansion Headers
GF AIF4RXDAT/BCLK/TXDAT/LRCLK	0x70 - 0x73	Connects to the GF AIF4 pins on the underside Expansion Headers
GF AIF1RXDAT/BCLK/TXDAT/LRCLK	0x74 - 0x77	Connects to the GF AIF1 pins on the underside Expansion Headers
GF AIF2RXDAT/BCLK/TXDAT/LRCLK	0x78 - 0x7B	Connects to the GF AIF2 pins on the underside Expansion Headers
Codec PDMCLK/DATn	0x90 - 0x93	Connects to the PDM signals on the Codec Minicard
Codec DMICCLK/DATn	0xA0 - 0xA7	Connects to the DMIC signals on the Codec Minicard
DSP DMICCLK/DATn	0xA8 - 0xAB	Connects to the DMIC signals on the DSP Minicard
DSP UARTn RX/TX	0xC0 - 0xC3	Connects to the UART signals on the DSP Minicard
GF UARTn RX/TX	0xC4 - 0xC5	Connects to the UART signals on the underside Expansion Headers
USB UART RX/TX	0xC6 - 0xC7	Connects to the UART signals coming from the USB interface
External JTAG TCK/TDI/TRST N/TDO	0xD0 - 0xD4	Connects to the JTAG signals coming from the External JTAG Header
USB JTAG TCK/TDI/TMS/TRST N/TDO	0xD5 - 0xD9	Connects to the JTAG signals coming from the USB interface
I2Cn SCL/SDA	0xE0 - 0xE5	Connects to the various I2C buses on the Lochnagar 2 system
Logic 0	0xFE	Applies a logic '0' signal
Logic 1	0xFF	Applies a logic '1' signal

11 JTAG

The Lochnagar 2 has JTAG debugging functionality built in through the USB interface, and does not require any third party adapters for on-chip debugging of ADSP2 cores. The JTAG header J1 is still present on the Lochnagar 2 board, so it is still possible to use an external controller such as the Macraigor usb2Wiggler™ if required.

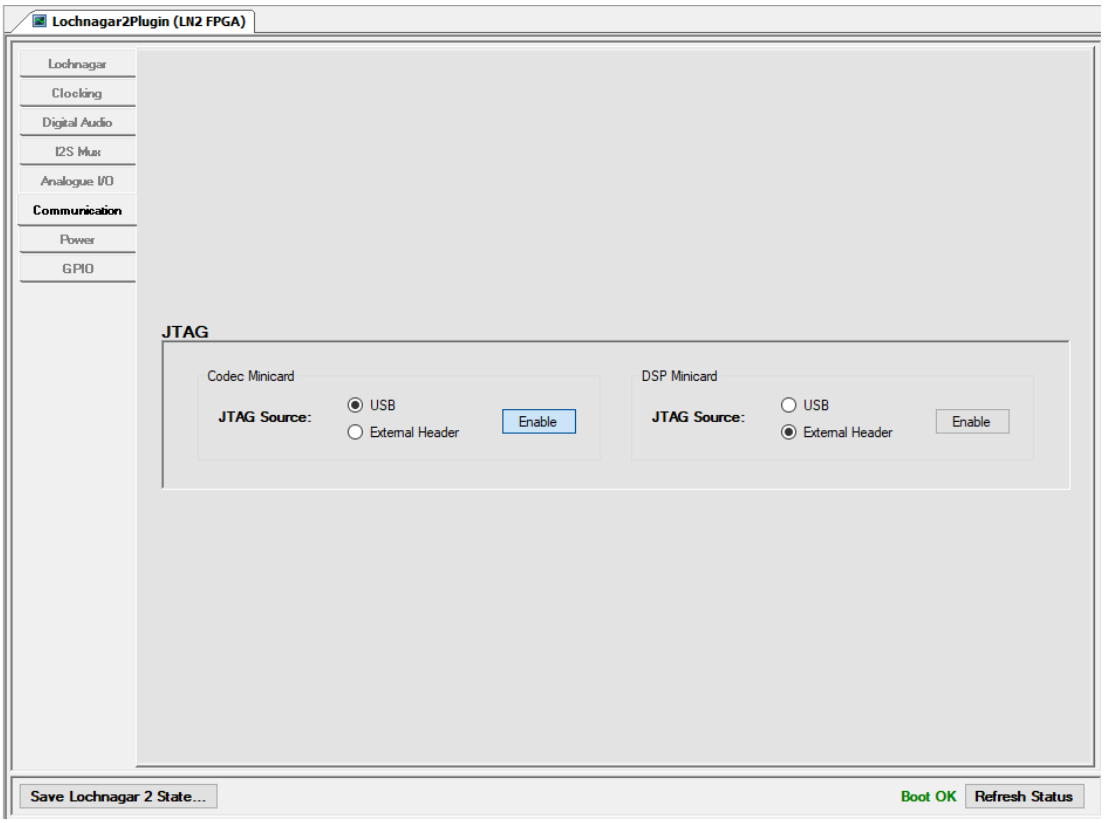
11.1 Required Chess toolchain update

Some machines in combination with some versions of the Synopsys Chess toolchain may have trouble connecting JTAG on Lochnagar 2 platforms. In this situation, ChessDE always reports that the PM0 contents are 0xFFFFFF.

If observed, it is recommended to update to the latest version of the Synopsys Chess toolchain.

11.2 JTAG configuration

JTAG settings on Lochnagar 2 are configured via the **Communication** panel on the Lochnagar 2 Plugin.



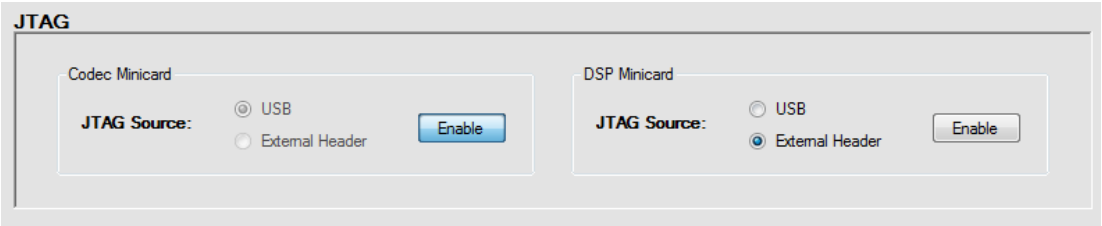
JTAG can be sourced from one of two sources:

- USB: JTAG interface to computer via the Lochnagar 2 USB cable
- External Header: 14-pin J1 "JTAG" header at top of Lochnagar 2 board. This can be used with standard JTAG dongles such as Macraigor usb2Wiggler (U2W-ONCE variant)

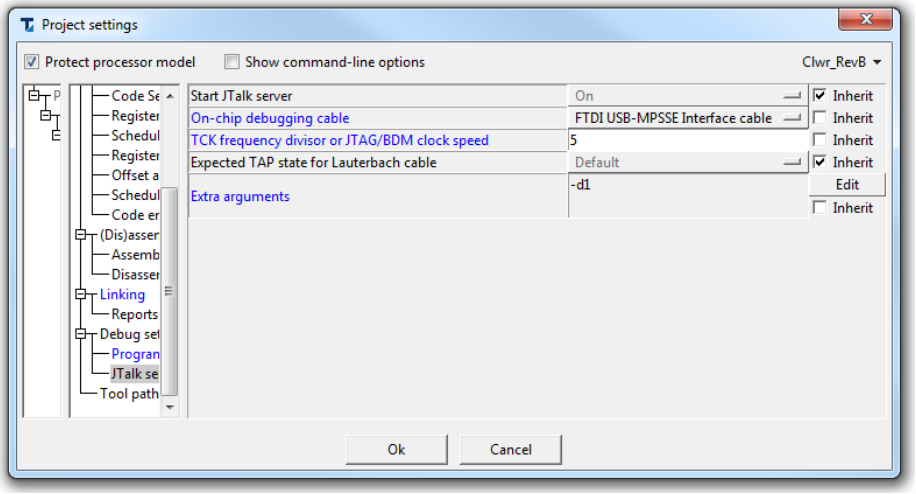
JTAG can be used to debug DSP cores on either of the Codec or DSP minicard headers. The same JTAG source cannot be used for both Codec and DSP minicard devices.

11.2.1 Example configuration

1. Make sure that the Lochnagar 2 board is connected to the PC via the USB cable.
2. Enable JTAG from USB to the Codec minicard in the Lochnagar 2 plugin:

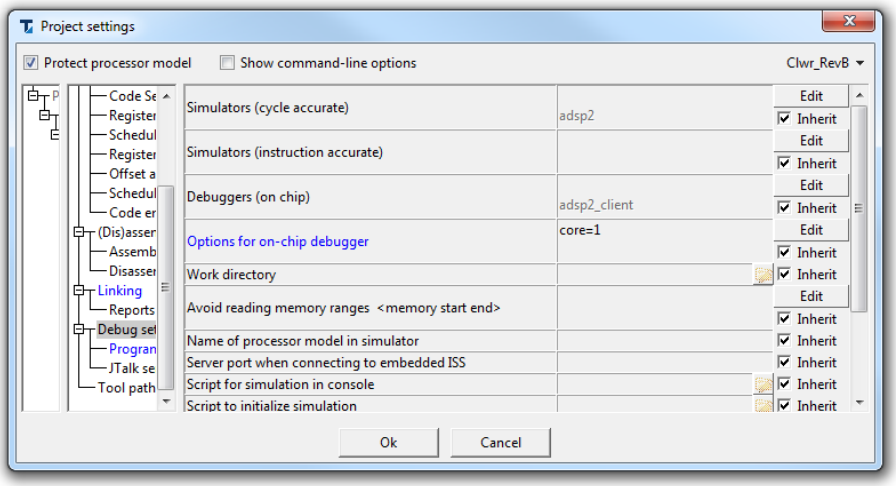


3. In the Chess Project settings, select the FTDI USB-MPSSE Interface cable, a TCK frequency divider of 5, and an extra argument of -d1.



4. Rebuild the Chess project and download it to the Cirrus Logic Smart Codec device in the usual way.
5. Ensure the debug clock is enabled on the Cirrus Logic Smart Codec device, and that the core is programmed and running.
6. It should now be possible to start debugging from the ChessDE environment in the usual way.

The correct core must be specified in the Chess 'Debug settings' menu. This is done by specifying 'core=n', where n is the core number from 1-7. Make sure that the build configuration in the top-right corner is set to the correct chip, rather than <All>. If not specified, Chess will default to debugging core 1.

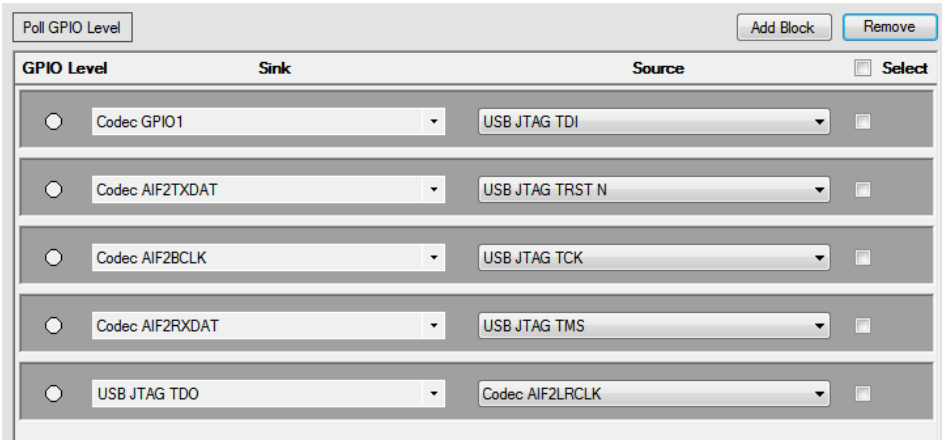


11.3 Custom JTAG Pin Configurations

The controls on the **Communications** panel of the Lochnagar 2 Plugin assume that the JTAG functionality on the Cirrus Logic minicard will have a dedicated set of JTAG pins for debugging purposes. However, on some devices, the JTAG functionality shares the same physical pins as other digital peripherals on the chip, such as the digital audio interfaces. In these scenarios, some additional configuration is required.

In these scenarios, the **GPIO** panel of the Lochnagar 2 Plugin must be used to configure the custom pin mapping.

For example, if the JTAG pins on the Cirrus Logic minicard are multiplexed with the Codec AIF2 pins (and Codec GPIO1), the following settings would connect the USB JTAG interface to the devices on the Cirrus Logic minicard:



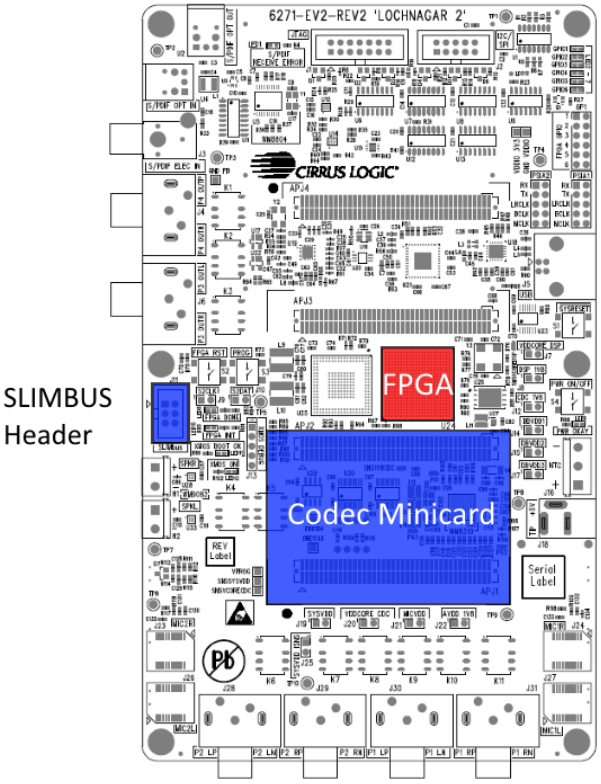
Note that the TDI, TRST N, TCK and TMS signals are inputs to the device, TDO is an output and is routed in the opposite direction. GPIO options are also available for use with the External JTAG Header. These settings will override the standard pin mappings used by the **Communications** panel. Note that the appropriate USB or External "Enable" button must still be selected on the **Communications** page for JTAG communications to work.

12 SLIMbus

Cirrus Logic Smart Codec devices on Lochnagar 2 can be controlled using the SLIMbus protocol.

SLIMbus is an interface protocol that can be used for both control (i.e. writing to the codec register map) and audio transport. It is a very flexible protocol which can be changed dynamically to facilitate high and low bandwidth traffic as efficiently as possible. With mutliline SLIMbus, this is further improved with extra data lines specifically used for data transport, as well as other updates/features to improve firmware transfer rates.

Lochnagar 2 does not natively support this format through USB. Third-party equipment must be used to connect through the J11 "SLIMbus" header on the board. An Application Processor connected to the Expansion Headers on the underside of Lochnagar 2 can also use the SLIMbus protocol to communicate with the Smart Codec.



12.1 SLIMbus Header

The signals from the SLIMbus Connector J11 are routed directly to the codec minicard and can be used to control it directly.

No additional register configuration is required on the Lochnagar 2 board to enable this.

J11 Pin	Signal
1	SLIMCLK
2	GND
3	SLIMDAT
4	GND
5	n/c
6	GND

12.2 SLIMbus through Expansion Headers

The expansion headers on the underside of Lochnagar 2 are connected to the codec minicard SLIMbus signals. If an Application Processor that supports the SLIMbus protocol is connected to the Lochnagar 2 expansion headers, it can be used to control the Smart Codec via this interface.

No additional register configuration is required on Lochnagar 2 to enable this.

13 Power

The Lochnagar 2 provides a level of configuration for the power supply rails on the board.

13.1 Automatic Power Configuration

The Lochnagar 2 board will automatically detect and configure the power rails on the board appropriately based upon the minicards it detects. If no minicards are connected, the default value for all configurable voltage rails is 0 V.

Depending on the requirements of the particular minicards connected, the codec and DSP core voltage rails will be automatically set to one of the following values:

- 1.2 V
- 0.9 V
- 0 V

This configuration is done automatically and does not require any user interaction through the plugin or register map. The automatic trim feature may or may not be enabled depending upon the minicard requirements. Changes made to these values through the register map or plugin will not persist through board power cycles or soft resets, which will restore the voltage rails back to the appropriate default values for the attached minicards.

Applying an incorrect voltage to the core rail may permanently damage the Cirrus Logic devices on the attached minicards. The ability to configure the voltage levels of the core voltage rails is an advanced feature for power users only.

If there is a problem identifying one of the connected minicards, or if two or more of the connected minicards have conflicting voltage rail requirements, the system will not power up any of the configurable rails to avoid accidentally applying the wrong voltage to any of the connected devices. To see if there has been such a problem, check the SYS_STS field in the RESET_CTRL1 (R0Bh) register.

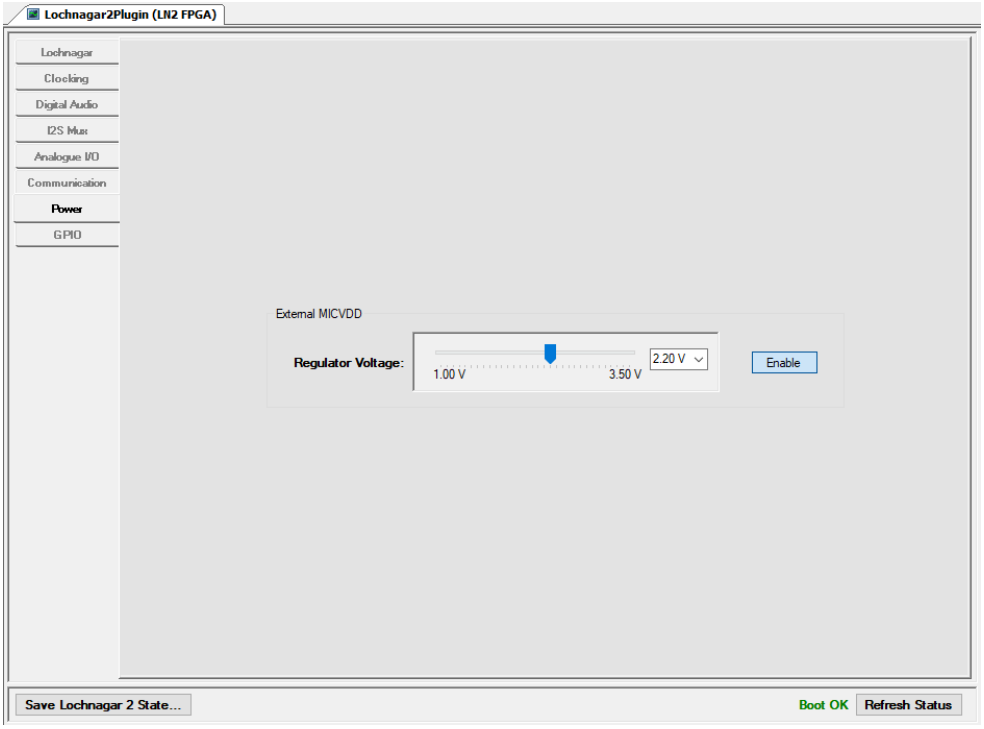
SYS_STS codes:

- Bit 3 = Conflict between minicard requirements. This means that the combination of minicards connected is not compatible and cannot be used together. This bit could also indicate that there was an error detecting one of the minicards.
- Bit 2 = Error detecting minicards. One of the minicards connected has not been correctly configured for the voltage rail self-configuration feature and should be returned to Cirrus Logic for fault finding.

The other bits in SYS_STS have other meanings that are not associated with the configurable voltage rails.

13.2 Configuring Power Options

The power rail options are configured through the **Power** tab of the Lochnagar 2 Plugin.



13.3 MICVDD Options

Most Cirrus Logic Smart Codec devices generate their own MICVDD voltages from an internal regulator and therefore this power rail is usually an output from the codec minicard.

However, some Smart Codecs do not have an internal regulator and require MICVDD to be supplied as an input to the chip. Lochnagar 2 provides the option to generate a voltage on the MICVDD rail and supply it to the chip. The voltage can be configured as any value between 1.00 V and 3.50 V, stepping in 0.05 V increments between 1.00 and 1.60 V and 0.1 V increments between 1.60 and 3.50 V.

13.3.1 Example Configuration

To configure the MICVDD voltage:

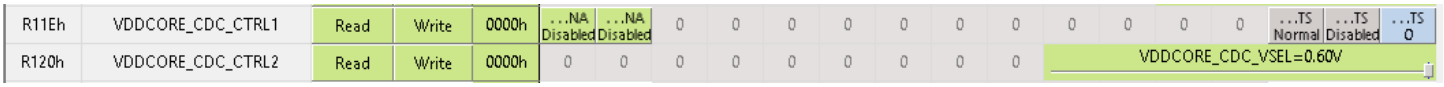
1. Navigate to the **Power** tab of the Lochnagar 2 Plugin.
2. Select the desired voltage level from the slider / drop-down menu.
3. Click the "Enable" button to supply this voltage on the MICVDD rail.

MICVDD should only be enabled on the Lochnagar 2 for devices that do not generate their own MICVDD voltage internally.

13.4 VDDCORE Codec Options

It is sometimes useful to disable the core voltage for the codec in order to enter low power sleep modes. If the core supply is provided by an internal regulator on the chip itself, this can be done by register writes to the device. For devices that do not have an internal regulator, or use cases which do not use it, the external voltage rail must be powered down to achieve the same effect. Lochnagar 2 provides the ability to power down its external codec core voltage rail using the Lochnagar 2 register map. It is also possible to change the voltage level on this rail, but this is not recommended as an incorrect voltage level may permanently damage the devices on the Lochnagar 2 minicards.

Currently there is no plugin interface to provide this functionality. These changes must be made at the register map level.



Note that the Lochnagar 2 board determines an appropriate default setting for these registers based upon the minicards it has detected, so that the core voltage is set appropriately for the devices that are connected. It is not recommended to change this voltage from the default value, as this may permanently damage the Cirrus Logic devices on the connected minicards.

R11Eh (VDDCORE_CDC_CTRL1) contains:

- VDDCORE_CDC_REG_ENA (bit 15) = enable switch for the VCCCORE_CDC rail
- VDDCORE_CDC_TRIM_ENA (bit 14) = enable automatic voltage trim
- VDDCORE_CDC_REG_UV_STS (bit 2) = status flag for under-voltage error
- VDDCORE_CDC_REG_STS (bit 1) = status flag for register enable status
- VDDCORE_CDC_REG_UPDATE_STS (bit 0) = pulse a logic 1 to this bit in order to force an update of the status flag bits

R120h (VDDCORE_CDC_CTRL2) contains:

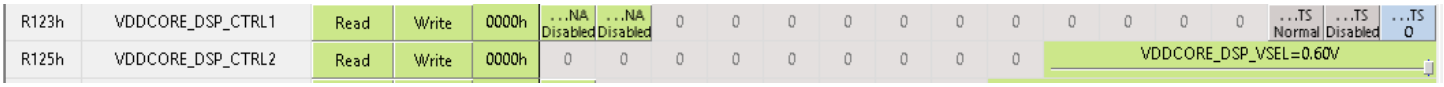
- VDDCORE_CDC_VSEL (bits 4:0) = sets voltage level for the VDDCORE_CDC rail from 0.6 V to 1.3125 V in 12.5 mV steps. 00-08h = 0.6 V, 09h = 0.6125 V etc.

The voltage trim enable bit is normally set depending on the minicard requirements and it is not recommended to change this from the default. If trim is enabled, the Lochnagar 2 will use feedback to ensure that the voltage on the rail is as close to the selected VSEL value as possible. If the trim enable is set, this action will be performed during Lochnagar 2 board initialization or when the voltage rail is enabled in the register map. If the rail is already enabled when the trim bit is set the trim action will be performed immediately, during which the rail will be disabled and re-enabled several times. On a soft reset of the Lochnagar 2 board, the voltage rail settings will be restored to the original trim value calculated when the board was first powered on. It is recommended that the minicard device is held in reset when the trim is being performed for best results.

13.5 VDDCORE DSP Options

Similar to the VDDCORE Codec rail, it is sometimes advantageous to power down the VDDCORE DSP rail for power saving reasons. Lochnagar 2 provides the ability to power down its external DSP core voltage rail using the Lochnagar 2 register map. It is also possible to change the voltage level on this rail, but this is not recommended as an incorrect voltage level may permanently damage the devices on the Lochnagar 2 minicards.

Currently there is no plugin interface to provide this functionality. These changes must be made at the register map level.



Note that the Lochnagar 2 board determines an appropriate default setting for these registers based upon the minicards it has detected, so that the core voltage is set appropriately for the devices that are connected. It is not recommended to change this voltage from the default value, as this may permanently damage the Cirrus Logic devices on the connected minicards.

R123h (VDDCORE_DSP_CTRL1) contains:

- VDDCORE_DSP_REG_ENA (bit 15) = enable switch for the VCCCORE_DSP rail
- VDDCORE_DSP_TRIM_ENA (bit 14) = enable automatic voltage trim
- VDDCORE_DSP_REG_UV_STS (bit 2) = status flag for under-voltage error
- VDDCORE_DSP_REG_STS (bit 1) = status flag for register enable status
- VDDCORE_DSP_REG_UPDATE_STS (bit 0) = pulse a logic 1 to this bit in order to force an update of the status flag bits

R125h (VDDCORE_DSP_CTRL2) contains:

- VDDCORE_DSP_VSEL (bits 4:0) = sets voltage level for the VDDCORE_DSP rail from 0.6 V to 1.3125 V in 12.5 mV steps. 00-08h = 0.6 V, 09h = 0.6125 V etc.

The voltage trim enable bit is normally set depending on the minicard requirements and it is not recommended to change this from the default. If trim is enabled, the Lochnagar 2 will use feedback to ensure that the voltage on the rail is as close to the selected VSEL value as possible. If the trim enable is set, this action will be performed during Lochnagar 2 board initialization or when the voltage rail is enabled in the register map. If the rail is already enabled when the trim bit is set the trim action will be performed immediately, during which the rail will be disabled and re-enabled several times. On a soft reset of the Lochnagar 2 board, the voltage rail settings will be restored to the original trim value calculated when the board was first powered on. It is recommended that the minicard device is held in reset when the trim is being performed for best results.

14 Current Monitor

Lochnagar 2 features built-in Current Monitor circuitry that allows for the measurement of both voltage and current on up to eight of the supply voltage rails provided to the minicards. The Current Monitor does not require any hardware modifications or external circuitry to operate. The current and voltage measurements are obtained through the standard register map interface to the Lochnagar 2 FPGA, and can therefore be monitored by software.

14.1 Lochnagar 2 Power Rails

The current monitor is provided for indication purposes only and not as an absolute measurement.

All rails are accurate to roughly 1% for all measurements above 1 mA.

For greater accuracy, a removable jumper is provided on each rail to allow for the serial insertion of an external multimeter.

14.1.1 Monitored Voltage Rails

Channel	Rail	Minicard	Jumper	Notes
1	DBVDD1	Codec	J14	
2	1V8 DSP	DSP / Codec	J8	
3	1V8 CDC	Codec	J12	
4	VDDCORE DSP	DSP / Codec	J7	
5	AVDD 1V8	Codec	J22	
6	SYSVDD	Codec	J25	• It is not possible to measure voltage on the SYSVDD rail. • Current measurements on the SYSVDD rail have a fixed offset that varies from board to board. It is recommended to calibrate SYSVDD current measurements by measuring the current with no minicard connected to determine this offset, or by connecting an external multimeter to verify.
7	VDDCORE CDC	Codec	J20	
8	MICVDD	Codec	J21	• Voltage monitor readback saturates at 2.5 V, although this rail is capable of running up to 3.3 V.

The channel number determines the order that the rails are displayed within the Current Monitor plugin and is used by the register interface to trigger readings on each of the rails.

The minicard column shows which minicard type this power rail can power. The DSP power rails can also be used by 3-header Codec cards that span headers APJ1 to APJ3. Note that not all minicards will use all the available power supplies, and that sometimes minicard schematic designers may choose to connect various supply rails together. For example, the DBVDD1 supply rail from Lochnagar may be left disconnected on the minicard if the designer has chosen to connect the Smart Codec's DBVDD1 pin to the generic 1V8 CDC rail instead.

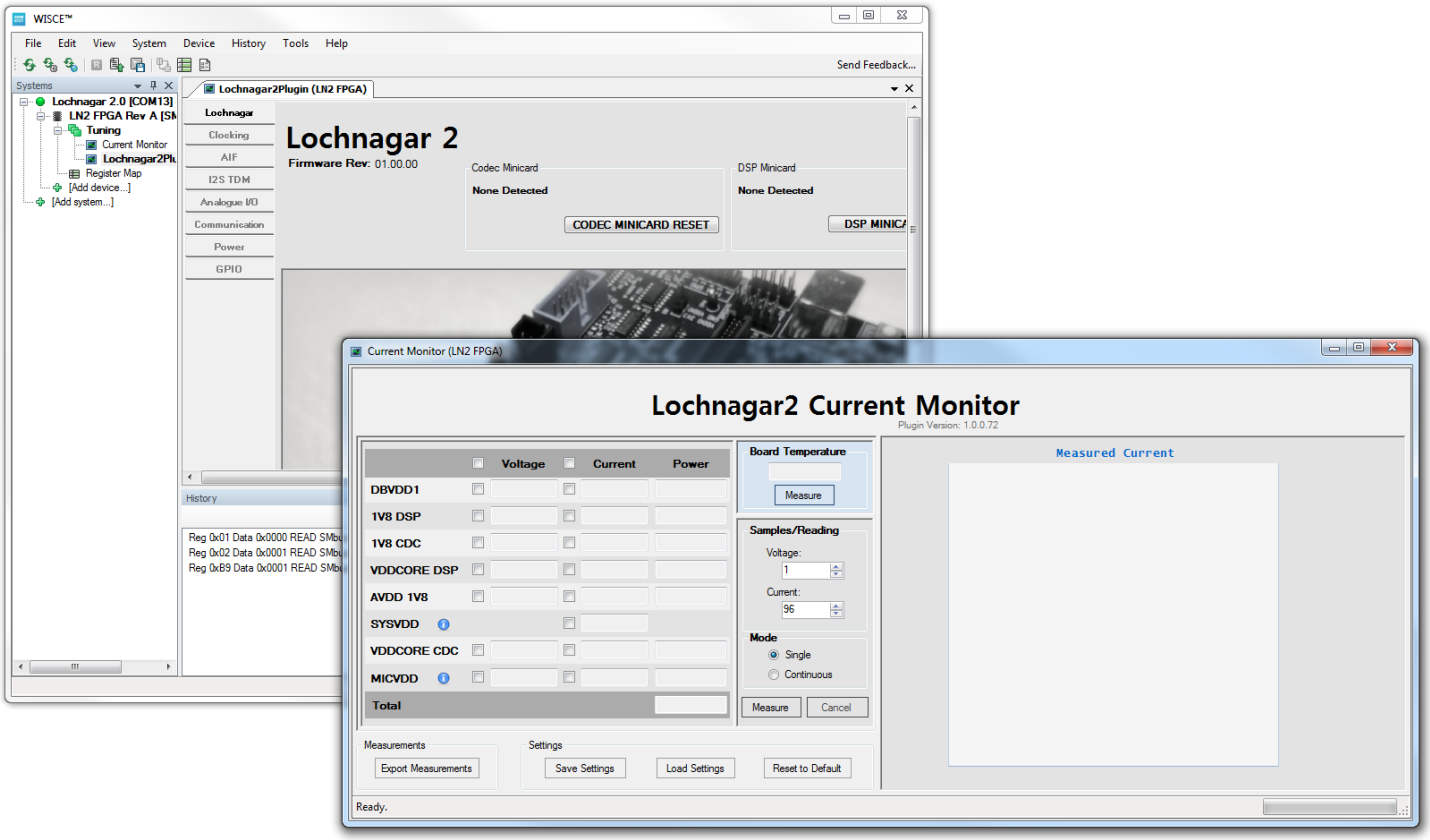
14.1.2 Unmonitored Voltage Rails

There is no provision to monitor the following voltage rails using the built-in Current Monitor. To measure current on these rails, remove the appropriate jumper and insert a digital multimeter in serial between the two pins of the jumper header.

Rail	Minicard	Jumper
DBVDD2	Codec	J15
DBVDD3	Codec	J17

14.2 Current Monitor Plugin

The Current Monitor is accessed through the Lochnagar 2 Register Map. The interface requires a complex sequence of register writes in order to trigger and interpret measurements, so this has been simplified by providing a plugin interface.The **Current Monitor** plugin appears separately from the main **Lochnagar2Plugin**. Having them separate allows the user to undock and view the two plugins simultaneously. Both are installed by the Lochnagar 2 Device Pack can be accessed from the "Tuning" folder of the LN2 FPGA device in the WISCE™ Systems tree.



14.2.1 Voltage / Current Rail Selection

Two checkboxes are provided for each of the measureable rails: one for measuring voltage, the other for current. At the top of each column, there is an additional checkbox that allows all voltages or current checkboxes to be selected/deselected in a single click.

When a measurement is triggered in either Single or Continuous mode, the current monitor plugin measures all currents and voltages that are currently checked. The operation will take longer when more checkboxes are ticked.

14.2.2 Power Measurement

If both Voltage and Current measurements are selected for the same rail, the plugin calculates the power consumed on that rail by multiplying the values together. It also automatically sums all of the calculated power values into a total, displayed underneath the table. This applies to both Single and Continuous measurement modes.

14.2.3 Measurement Modes

14.2.3.1 Single

In Single Measurement Mode, pressing the "Measure" button triggers a single measurement of all voltages and currents that are currently checked. The values are displayed in the boxes next to the checkbox. Graphing is disabled in Single Measurement Mode.

14.2.3.2 Continuous

In Continuous Measurement Mode, the "Measure" and "Cancel" buttons change into "Start" and "Stop" buttons. The Current Monitor plugin repeatedly triggers measurements of all selected voltages and currents until the "Stop" button is pressed. When in continuous measurement mode, the plugin also charts the selected current measurements on a graph for ease of visibility over time. The refresh rate of the measurements/graph depends on how many currents and voltages are being simultaneously measured.

14.2.4 Samples/Reading

These parameters control the filtering performed by the current measurement circuitry, and determine how many raw samples are required in order to obtain one voltage or current measurement. Each parameter is in the range 1-1023. The higher this number, the more samples are used to produce a voltage or current measurement value. High numbers will result in slower but more precise measurements. Low values will result in faster but less precise measurements.

The recommended default values for the Samples/Reading settings are:

Measurement Type	Default S/R
Voltage	1
Current	96

14.2.5 Export Measurements

The Export Measurements button will save measurement data from the plugin as a Comma Separated Values (CSV) file that can be opened in a spreadsheet or text editor.

In Single Mode, the CSV file will contain the current set of measurements displayed on the screen, including the Samples/Reading settings, board temperature (if measured) and all currently selected voltage and current readings. If both voltage and current are present it will also save the calculated power measurements and total as displayed on the plugin page.

In Continuous Mode, the CSV file will contain the complete list of measurements taken since the continuous measurement started. The start of the file will list the Samples/Reading settings and board temperature (if measured). Each row after this will contain a timestamp followed by a column for each of the currently selected voltage and current readings. The timestamp is taken after all measurements on that row have been completed. Whilst continuously operating the plugin will store up to 10 megabytes of measurement data for export, after which it will delete the oldest 500 kilobytes of measurements to make space for new data as and when required.

14.2.6 Save/Load/Restore Settings

The Current Monitor plugin automatically stores the current configuration (selected checkboxes, samples/reading settings and measurement mode) as an XML file and automatically restores them the next time the plugin is opened. This means that the user does not have to re-select their desired current or voltage rails every time the WISCE™ application is opened. The "Save Settings" button allows the user to save a copy of the XML file to their hard drive in order to share it with others, or quickly switch between different Current Monitor configurations. The "Load Settings" button allows the user

to load in a previously saved XML file to restore those settings. The "Restore to Default" button resets all options in the plugin back to their default values.

14.2.7 Board Temperature

Press the "Measure" button to perform a temperature measurement on the Lochnagar 2 board.

The temperature is measured by U41 on the underside of Lochnagar 2. The measurement capability of this chip is accurate to +/- 2 degrees Celsius.

15 Example Setup Scripts

This page details the example setup scripts provided as part of the WISCE™ Device Pack. Scripts are not backwards/forwards compatible between Lochnagar 2 and the original Lochnagar board.

15.1 WISCE™ Profile Scripts

A WISCE™ Profile Script is a text file containing a sequence of register reads and writes. Each line of the text file contains a separate register read or write command. Profile Scripts are used to automate chip setup for Cirrus devices, to replicate existing setups and/or return the board to a known configuration.

Profile Scripts can:

- Write to multiple devices on the system
  - For example, the same profile script can write to registers on a Cirrus Logic Smart Codec device and also to the Lochnagar 2 FPGA.
- Recursively call other Profile Scripts
  - For example, a common set up of Lochnagar 2 FPGA setup scripts can be called by a variety of higher level scripts that configure both the LN2 board and codec device.

The WISCE™ Profile Scripts provided with the Lochnagar 2 WISCE™ Device Pack are installed automatically to the following directory:

```
C:\Program Files (x86)\Wolfson Evaluation Software\Profiles\Lochnagar2
```

Assuming that the WISCE™ application has been installed to the default installation directory. The "Profiles" folder of the WISCE™ installation directory should be the default search path when the user clicks on *File->Load..* within the WISCE™ application. Profile Scripts are run from within WISCE™ by clicking on *File->Load...* and selecting the appropriate Profile Script text file.

15.2 Lochnagar 1 and Lochnagar 2 Register Compatibility

Lochnagar 2 registers are in a different format to the registers of the original Lochnagar board, so scripts are not forwards/backwards compatible.

The scripts included with the Lochnagar 2 Device Pack use a new WISCE™ feature to detect whether a Lochnagar 1 or Lochnagar 2 board is connected and load a different sub-script depending on which board is present. This feature allows the top level profile script to read register 0x00 of the Lochnagar device (at I2C address 0x44) and load a different lower level FPGA configuration script depending on whether Lochnagar 1 or Lochnagar 2 is connected. An example is shown below:

```
  * If Lochnagar 1 (ID = 0x50) is present at register 0x00 address 0x44, then load the
spdif_to_cdc_aif1.txt file
  * Otherwise load L2_spdif_to_cdc_aif.txt

  IF 0x00 0x50 SMbus_8_bit_data CHECK 0x44 0xFF
  LOAD spdif_to_cdc_aif1.txt
  ELSE
  LOAD L2_spdif_to_cdc_aif1.txt
  ENDIF
```

This feature was introduced in WISCE™ 3.4.0.19. The profile scripts provided with the Lochnagar 2 Device Pack will generate an error on previous versions of WISCE™, as they do not understand the IF/ELSE syntax.

15.3 Details of Scripts Provided

The scripts provided with the Lochnagar 2 Device Pack are split into two types.

15.3.1 Configuration Template Script

The configuration template file provides a blank template for configuring a full system including both a Lochnagar board and a Smart Codec minicard. It detects whether the system is using a Lochnagar 1 or Lochnagar 2 and allows the user to load a sub-script based upon this detection. The file then provides commented sections to illustrate the normal sequence for setting up registers in a Cirrus Logic Smart Codec.

Note that specific example scripts for setting up particular Smart Codecs are provided along with the WISCE™ Device Pack for that Smart Codec device.

Name of Script	Description
Configuration_Template.txt	Configuration Template for Smart Codec Setup This file illustrates the normal sequencing for initializing a Lochnagar based platform with a Cirrus Logic Smart Codec device. The file consists of commented sections which show the generic order of configuration. The file does not contain any register writes to the Smart Codec and is intended to be filled in as a template by the end user. The sections are: 1. Lochnagar: This section will call either a Lochnagar 1 or Lochnagar 2 setup script depending on which board is detected. This illustrates how the branching feature of WISCE™ profile scripts can be used to support both hardware platforms. 2. Patch File (if required) 3. Clocking configuration 4. Power management (MICBIAS) 5. Input enables 6. Digital audio enables 7. Mixer setup 8. Download DSP firmware 9. Output setup It is not required to fill in all sections. For example, if there is no DSP required in the intended use case, it is not necessary to download any firmware to the DSP cores in section 8.

15.3.2 Lochnagar Setup Scripts

The Lochnagar 1 and Lochnagar 2 setup scripts are usually loaded by top-level system configuration scripts such as the configuration template, and may be re-used in various Smart Codec use cases. It is intended that the end user use the WISCE™ plugin to create their own setup scripts for custom use cases if the example scripts do not meet their needs.

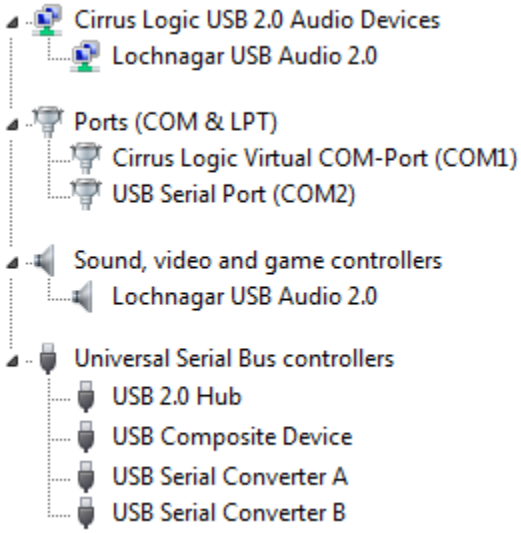
Name of Script	Description
L1_spdif_to_cdc_aif1.txt	**Lochnagar 1 configuration script.** *Should only be called when Lochnagar 1 board is detected.* Configures the Lochnagar 1 FPGA routing path for S/PDIF transceiver to AIF1 of the codec minicard. • Routes S/PDIF MCLK to Codec MCLK1 • Routes PMIC 32k Clock to Codec MCLK2 • Routes S/PDIF audio to Codec AIF1 and return path

Name of Script	Description
L2_spdif_to_cdc_aif1.txt	**Lochnagar 2 configuration script.** *Should only be called when Lochnagar 2 board is detected.* Configures the Lochnagar 2 FPGA routing path for S/PDIF transceiver to AIF1 of the codec minicard. • Routes S/PDIF MCLK to Codec MCLK1 • Routes PMIC 32k clock to Codec MCLK2 • Routes S/PDIF audio to Codec AIF1 and return path • Enables S/PDIF transceiver for optical input in hardware control mode
L2_usb_to_cdc_aif1.txt	**Lochnagar 2 configuration script.** *Should only be called when Lochnagar 2 board is detected.* Configures the Lochnagar 2 FPGA routing path for USB streaming to AIF1 of the codec minicard. • Routes USB MCLK In to Codec MCLK1 • Routes PMIC 32k clock to Codec MCLK2 • Routes USB AIF Channels[1-8] audio to Codec AIF1 and return path
L2_usb_to_cdc_aif1_stereo.txt	**Lochnagar 2 configuration script.** *Should only be called when Lochnagar 2 board is detected.* Configures the Lochnagar 2 FPGA routing path for USB streaming to AIF1 of the codec minicard. • Routes USB MCLK In (11/12MHz version) to Codec MCLK1 • Routes PMIC 32k clock to Codec MCLK2 • Routes USB AIF Channels[1-8] audio to I2S Mux • Routes I2S Mux stereo output channels[1-2] to Codec AIF1 • Routes return path from I2S Mux to USB AIF
L2_usb_to_soundcard.txt	**Lochnagar 2 configuration script.** Does not require a codec to be connected. Configures the Lochnagar 2 FPGA routing path for USB streaming to Sound Card (3.5 mm jacks on underside) • Routes USB MCLK to Sound Card MCLK • Routes USB AIF Channels[1-8] audio to Sound Card AIF and return path.

16 Troubleshooting

16.1 Lochnagar 2 Drivers in Device Manager

The Lochnagar 2 should appear as a number of devices in the Windows Device Manager.



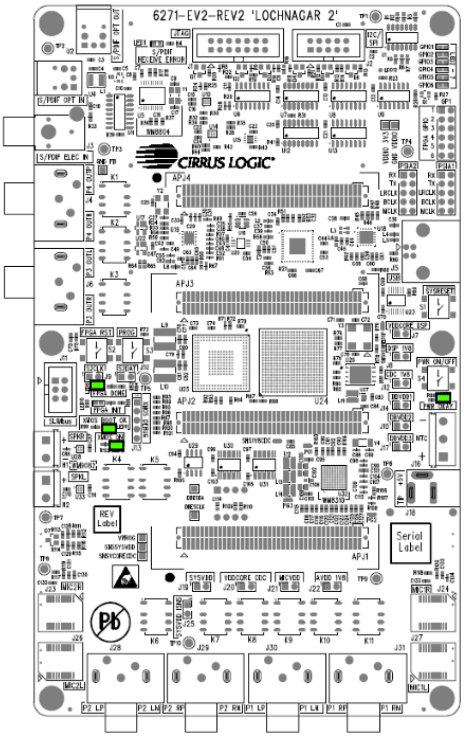
If any of these devices does not appear or appears in the Device Manager with a warning or error notification, the Lochnagar 2 board will not operate correctly.

16.2 Expected LED Configuration

If the board has booted correctly, the following LEDs are expected to be lit:

- LED8 (FPGA DONE)
- LED9 (PWR OKAY)
- LED11 (XMOS BOOT OK)
- LED12 (XMOS ON)

The following diagram shows the locations of these LEDs highlighted green.



If the board does not match this configuration, it could indicate that something has been corrupted in the board's firmware. It is therefore recommended to try the emergency firmware programming procedure detailed below.

16.3 Emergency Firmware Update Procedure

If the board LEDs are not in the correct configuration, this indicates there may be a problem with the board firmware. In this scenario, WISCE will not be able to detect the board and offer the prompt to update the firmware. For these scenarios, a command line version of the tools is provided within the WISCE installation folder, along with a batch file that can trigger the update process. Assuming WISCE has been installed in the default directory, the command line firmware update tools can be found in:

- *C:\Program Files (x86)\Wolfson Evaluation Software\Plugins\LochnagarSupportFiles*

Navigate to this folder and run the LN2_FirmwareUpdate_vXX.YY.ZZ.BBBB.bat batch file (where XX.YY.ZZ.BBBB matches the installed firmware version). This will trigger the firmware update process. The GPIO1-GPIO6 LEDs will flash while the board is updating, and it is important not to unplug the board or close the command line application while this is in progress.

If the firmware update batch file is not able to run or detect the board, the board may be physically damaged. In this instance, please contact your Cirrus Logic representative for a replacement.

16.4 Common issues with Lochnagar 2

This section will describe some of the more commonly observed issues with Lochnagar 2 and its drivers, and detail the solutions to these problems.

16.4.1 Installing new Device Pack causes Lochnagar 2 to stop responding

If the user installs a new version of the Lochnagar 2 Device Pack while audio is currently playing through the USB audio streaming functionality, the un-installation of the old audio drivers will require a machine reboot to complete. The driver installer cannot continue to install the new drivers until the old drivers have been removed, and it requires the user to manually restart the installation process after the machine reboot has completed. The error message presented by the audio driver installer is quite discreet and easy to miss.

In this scenario, the Lochnagar 2 will present itself in the Device Manager as a USB Composite Device with a warning message that indicates there are no drivers installed for the device.

Problem resolutions:

1. Stop audio playback and close all audio applications.
2. Run the Lochnagar 2 Device Pack installer again and ensure that the audio driver installation is successful. This may also require a full reset of the Windows Operating System.

This issue can be avoided by unplugging the board and closing all audio applications, JTAG debuggers and terminal applications that may have an open connection to the driver before starting the Device Pack installation.

16.4.2 Firmware update process causes Lochnagar 2 to stop responding

When performing a firmware update, the board should not be unplugged and the WISCE application should not be closed. The process will take between 3-5 minutes, during which the GPIO1-GPIO6 LEDs on the board will flash in a strobing pattern; while in this state it is dangerous to unplug the board or close the WISCE application, as this could cause the firmware to be corrupted and could cause the board to become unusable.

Sometimes the WISCE dialog box with the progress status can get hidden behind the main windows and it appears as if the application has stalled. Click the WISCE icon on the taskbar to make sure there are no additional windows open in the background. If WISCE appears to freeze while the board LEDs are flashing, wait for a minimum of 5 minutes (to give the firmware programming process a chance to finish) before attempting to rectify the situation.

If programming has been interrupted, it is likely that the board can no longer boot and the board LEDs will no longer light up in the expected pattern (see above). In this instance, there is an emergency reprogramming command line tool provided to attempt the programming steps again (see above).

16.4.3 COM Port Issue: Run out of COM port numbers

Each serial communication port in Windows is allocated with a unique COM port number. There are 256 available COM ports within Windows. Lochnagar 2 requires two separate COM ports: one Virtual COM port for communications with WISCE™, and a USB Serial Port that can be used for UART communications with Cirrus Logic devices that support the UART protocol. Windows will attempt to give each device a unique COM port number, so the Lochnagar 2 board will always be allocated the same COM port numbers. These numbers are now effectively allocated to this unique Lochnagar 2 board, and will remain allocated to it even when the board is not currently plugged in. If a different Lochnagar 2 board is plugged into the same system, it will be allocated a different set of COM port numbers.

It is possible for Windows to run out of available COM port numbers. In this instance, it will not be able to allocate COM port to one or both of the Lochnagar 2 COM port devices. In this instance, the affected COM ports will show a warning message in the Device Manager to indicate they are not operating correctly.

Problem resolutions:

1. Open the Device Manager and right-click on the affected COM/Serial Port.
2. Open the Properties dialogue.
3. In the Port Setting tab, click the "Advanced..." button to open another dialogue box.
   The Advanced Settings menu allows for manual selection of COM port from a drop-down menu. This will show which COM ports are currently available or marked as "(in use)".
4. Choose a COM port number from this list to allocate it to the Lochnagar 2 device.
   If the new selection is marked as "(in use)", a prompt box will ask for confirmation to continue. If the Lochnagar 2 COM port currently has a COM port assigned to it already, choosing a new COM port number will release its allocation on the old number, so by repeating this step it is possible to free up COM ports that are incorrectly marked as "(in use)"

16.4.4 Power cycling Lochnagar 2 while board is in use

There are several features of the Lochnagar 2 board that allow applications other than WISCE™ to connect to and communicate with the Lochnagar 2 board:

- USB audio streaming

- JTAG debugging via built-in JTAG port
- Serial terminal communcations with Lochnagar 2 UART

While using any of these features, it is not advisable to do any of the following actions:

- Power down the Lochnagar 2 board
- Unplug the Lochnagar 2 board
- Restart the Lochnagar 2 by pressing the SYSRESET button
- Restart the Lochnagar 2 by writing to the software reset register
- Update the firmware on the Lochnagar 2 board
- Undock laptop from docking station, disconnecting Lochnagar 2 from the PC

Power cycling the board in any of these ways whilst USB audio, JTAG debugging or UART serial communications are in progress will confuse the Lochnagar 2 board drivers, and may stop it from communicating correctly with WISCE™. This can be resolved with the following steps:

1. Close the application that is connected to Lochnagar 2 (USB audio, JTAG, UART) to stop the connection.
2. Close WISCE™
3. Power cycle the Lochnagar 2 board
4. Re-open WISCE™

Background Processes

Sometimes background processes, or processes that have become disassociated from their parent process, that have have been using the Lochnagar 2 USB subsystem can cause this problem (e.g. jtalk.exe). Make sure you close any such processes during step 1.

16.4.5 Lochnagar 2 still does not appear in WISCE™

This may have been caused by power cycling the Lochnagar 2 while the board was in use by another application, as described above. If the steps in the previous section do not resolve the issue, this may point to a driver issue with the COM ports.

To check for COM port driver issues:

1. Make sure both COM ports appear within the Device Manager as described in previous section.
2. Open the Windows regedit.exe application and find HKEY_LOCAL_MACHINE\HARDWARE\DEVICEMAP\SERIALCOMM. There should be two keys in this list associated with the Lochnagar 2 board: Device\USBSERxxx and Device\VCPx. The COM numbers on these serial ports should match up to the COM numbers observed in the Device Manager.

If one of the two COM ports is missing from the registry, Windows has encountered a USB serial driver error. To fix this:

1. Go to Device Manager and change the COM port number for the missing device.

The COM port should then correctly appear in both the Device Manager and the registry. If not, try switching the USB port that the Lochnagar 2 is connected to, as this will force Windows to re-configure the COM port drivers.

16.4.6 VDDCORE voltage rail is not powered up

Firmware version 1.1.0 introduced a new feature where the Lochnagar 2 board automatically detects which voltage rails are required for the particular minicards that are connected, as well as the required voltage level for those rails. It will then configure the power rails correctly for that particular minicard. This feature affects the following voltage rails on Lochnagar 2:

- MICVDD
- VDDCORE CDC

- VDDCORE DSP

These three rails will be disabled if there are no minicards connected, and will only be activated if one of the particular minicards requires that rail. All other voltage rails will be enabled by default. If there is a problem identifying one of the connected minicards, or if two or more of the connected minicards have conflicting voltage rail requirements, the system will not power up any of the rails to avoid accidentally applying the wrong voltage to any of the connected devices. To see if there has been such a problem, check the SYS_STS field in the RESET_CTRL1 (R0Bh) register.

SYS_STS codes:

- Bit 3 = Conflict between minicard requirements. This means that the combination of minicards connected is not compatible and cannot be used together. This bit could also indicate that there was an error detecting one of the minicards.
- Bit 2 = Error detecting minicards. One of the minicards connected has not been correctly configured for the voltage rail self-configuration feature and should be returned to Cirrus Logic for fault finding.

The other bits in SYS_STS have other meanings that are not associated with the configurable voltage rails.

17 Notices

The Lochnagar 2 audio drivers include ASIO Driver Technology by Steinberg Media Technologies.

ASIO is a trademark and software of Steinberg Media Technologies GmbH.

Aardvark is a trademark of TotalPhase, Inc.

LINUX is a registered trademark of Linus Torvalds.

SLIMbus is a trademark of MIPI Alliance, Inc.

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Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.